Carleton University
ELEC 4609A: Integrated Circuit Design and Fabrication
Static Logic PRSG Project Report
Group 19

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Chapter 1: IC Project Design

1.0 INTRODUCTION

The purpose of this project is to design, build, and test a chip that can produce an apparently random flash sequence. The complete project should fit within the layout shown in Figure 1.1, where λ = 2.4 microns. All measurements should be in increments of 2.4 microns.

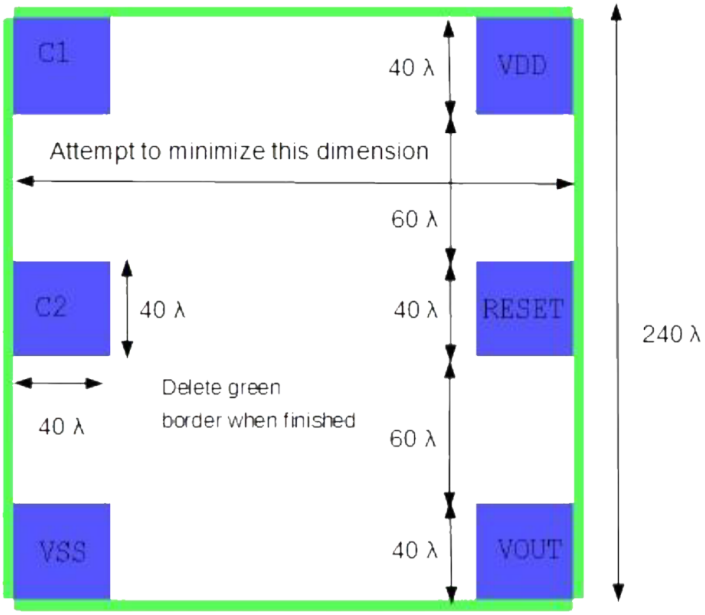


Figure 1.1: Probe pad placement for layout.

Pads C1 and C2 will connect a capacitor to a master clock generator within the chip. Pads VDD and VSS will connect to every pmos and nmos and must be routed through metal only. VOUT will output the pseudo random sequence and RESET will reset the sequence.

Requirements:

- Must fit within the area constraints
- Must generate a specific and reliable clock frequency (1ms)
- Pin locations
- Input Voltages (3V supply)
- VDD and VSS must route only through metal

2.0 SYSTEM DESIGN

The chip will produce a bit stream that appears random, but will repeat every 31 bits. Figure 1.2 shows a high level PRSG logic block diagram of the heart of the chip. There are five D flip flops and one XNOR gate with reset. It is also expected that the clock be generated using a master clock generator within the chip. This design is being used because it doesn't require a 2-phase clock generator and the d flip flops are not sensitive to off state leakage problems.

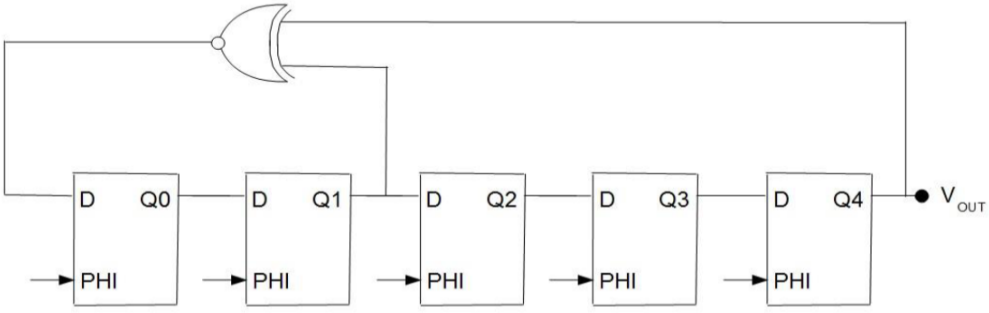


Figure 1.2: Pseudorandom sequence generator implemented with shift register and feedback.

Figures 1.3 and 1.4 show the XNOR gate with reset and the D flip flop.

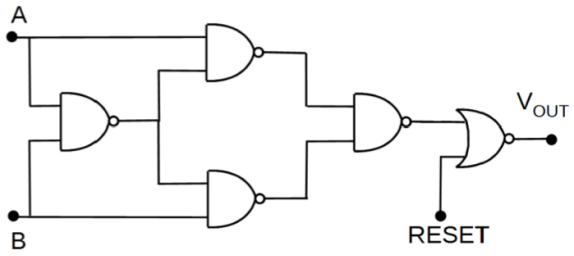


Figure 1.3: XNOR gate design with reset.

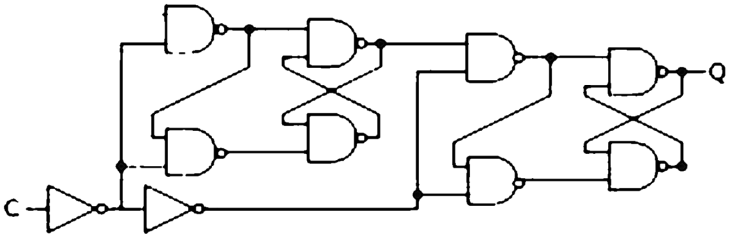


Figure 1.4: D flip flop design.

3.0 DESIGN OF INDIVIDUAL BLOCKS

3.1 Inverter

Inverters are NOT gates that will invert the input signals. Table 2 shows the expected output from all possible inputs. Note that the gate will have an inherent delay, so two inverters in series can act as a buffer.

Table 2: NAND gate truth table.

A	OUT
0	1
1	0

Figure 1.5 shows the inverter schematic design. The pmos has a length to width ratio of 0.25 and the nmos has a ratio of 0.50. The minimum wire width is set at 4.8 and the measurements must be in increments of 2.4u. Therefore, the pmos has a length of 4.8u and a width of 19.2u. The nmos has a length of 4.8u and a width of 9.6u.

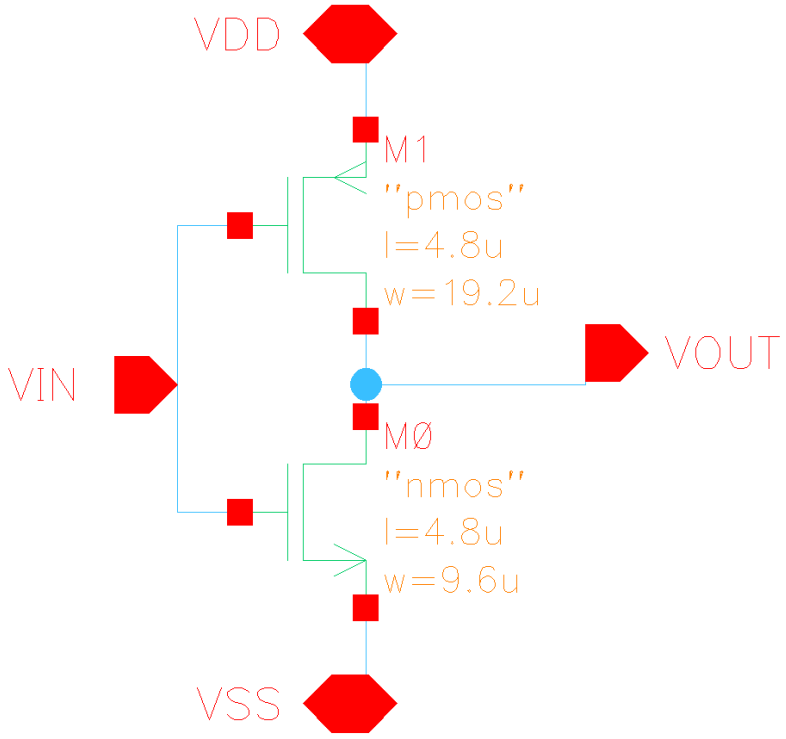


Figure 1.5: Inverter schematic design

Figure 1.6 shows the simulation results of the inverter schematic. These results are found to be successful. The pull-down time is 1ns and the pull-up time is 2 ns. Before the signals stabilise, the voltage peaks to well above the input values.

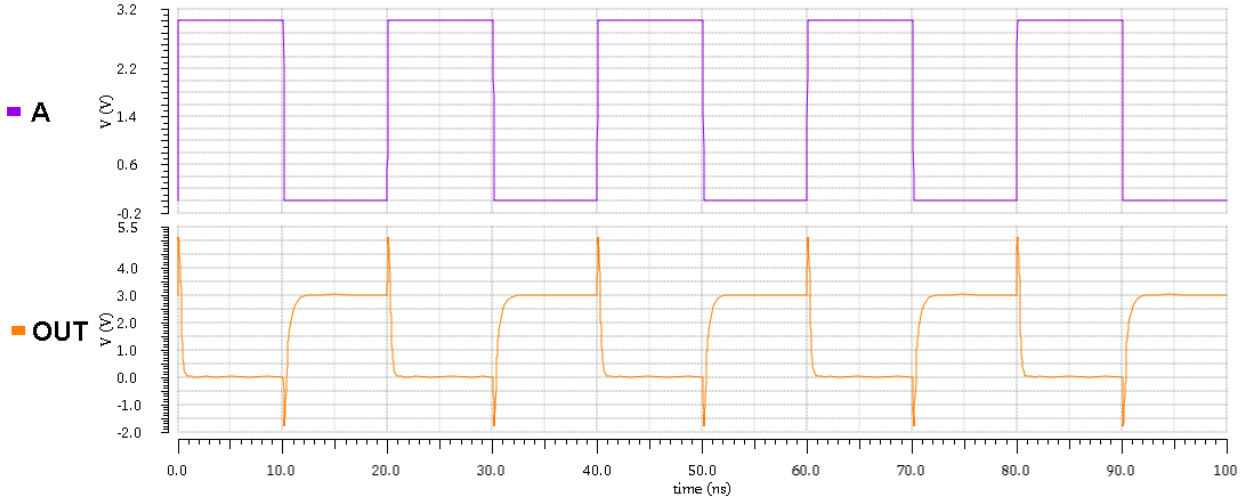


Figure 1.6: Inverter schematic simulation.

Figure 1.7 shows the inverter layout design. Since this gate is versatile and simple, multiple configurations were created to fit awkward space to maximise space. This layout is from the master clock generator.

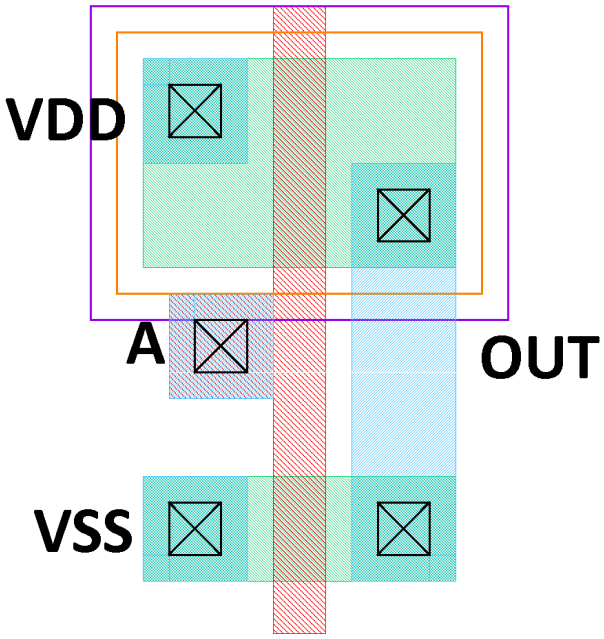


Figure 1.7: Inverter layout design.

3.2 NAND Gate

NAND gates will only output low if both inputs are high. Table 3 shows the expected output from all possible inputs.

Table 3: NAND gate truth table.

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure 1.8 shows the NAND gate schematic design. Each pmos has a length to width ratio of 0.25 and the nmos has a ratio of 0.25. The minimum wire width is set at 4.8 and the measurements must be in increments of 2.4u. Therefore, the pmos have a length of 4.8u and a width of 19.2u. The nmos have a length of 4.8u and a width of 19.2u.

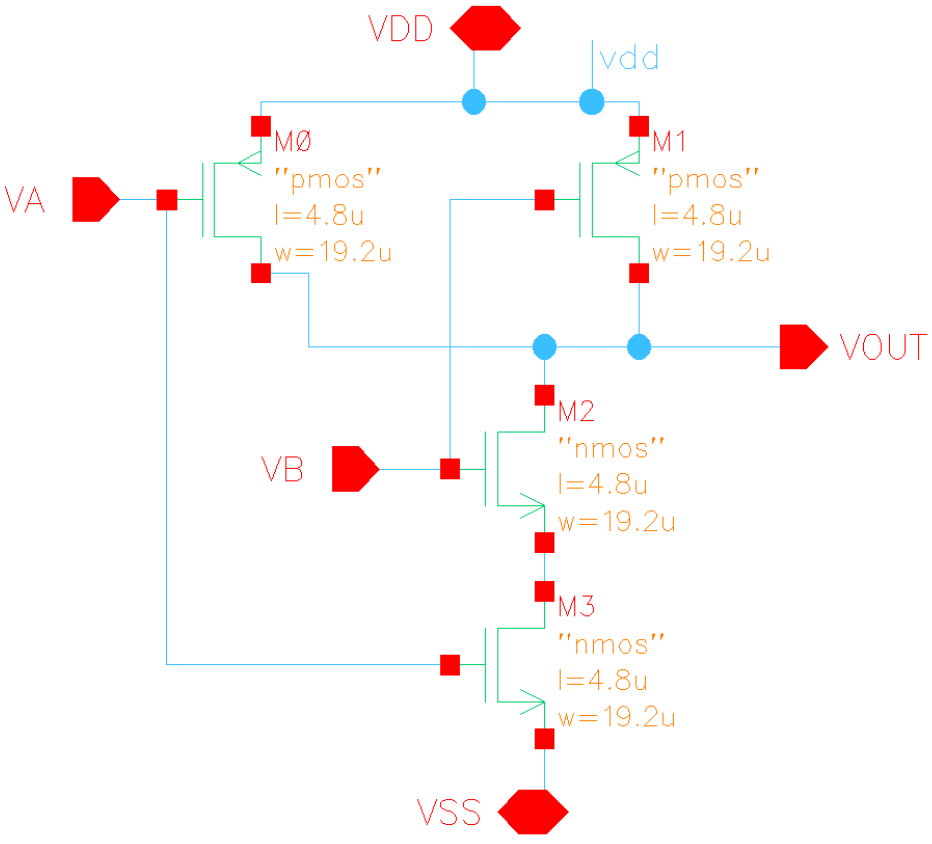


Figure 1.8: NAND gate schematic

Figure 1.9 shows the simulation results of the NAND gate schematic. These results are found to be successful. The pull-down time is 5ns and the pull-up time is 7ns. Before the signals stabilise, the voltage peaks to well above the input values.

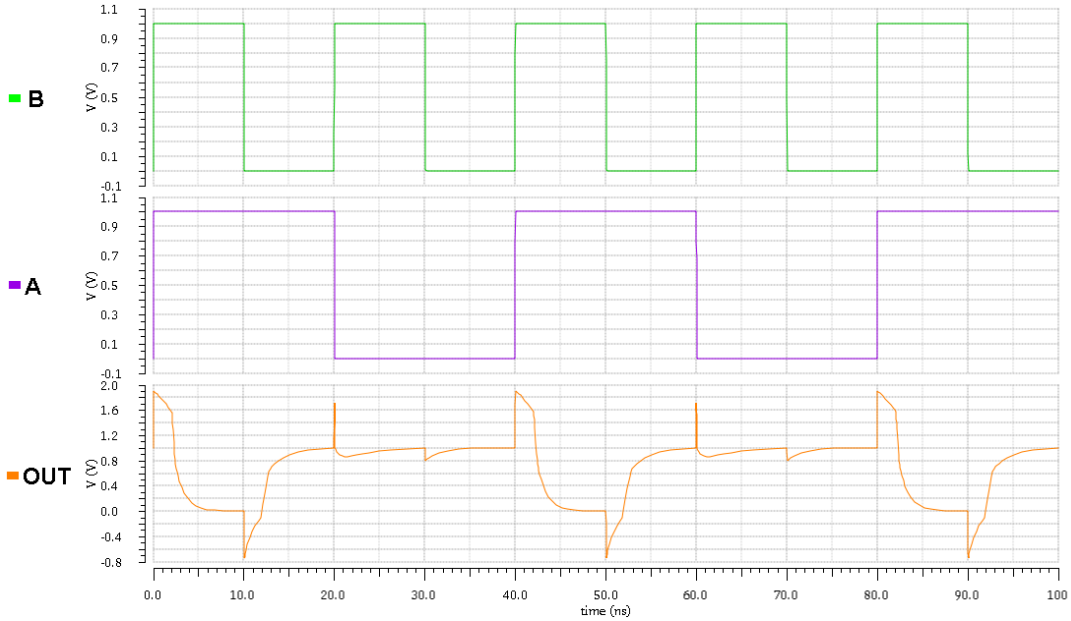


Figure 1.9: NAND gate schematic simulation results.

Figure 1.10 shows the NAND gate layout design. This layout is used throughout the chip.

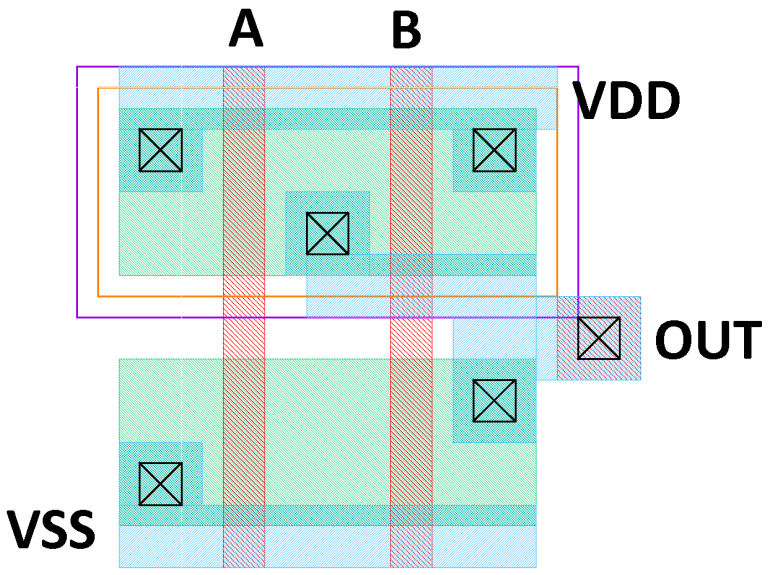


Figure 1.10: NAND gate layout design.

3.3 NOR Gate

NOR Gates will only output high if both inputs are low. Table 4 shows the expected output from all possible inputs.

Table 4: NOR gate truth table.

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1.11 shows the NOR gate schematic design. Each pmos has a length to width ratio of 0.125 and the nmos has a ratio of 0.50. The minimum wire width is set at 4.8 and the measurements must be in increments of 2.4u. Therefore, the pmos have a length of 4.8u and a width of 38.4u. The nmos have a length of 4.8u and a width of 9.6u.

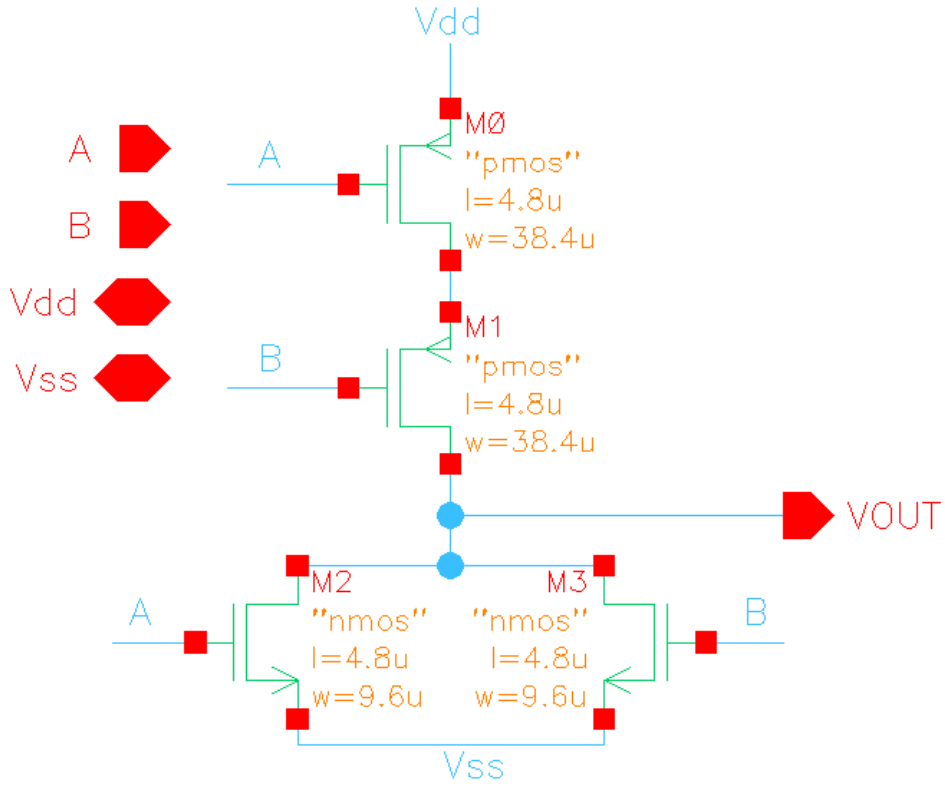


Figure 1.11: NOR gate schematic design.

Figure 1.12: shows the simulation results of the NOR gate schematic. These results are found to be successful. The pull-down time is 1ns and the pull-up time is 6ns. Before the pull-down signal stabilises, the voltage peaks to well above the input values.

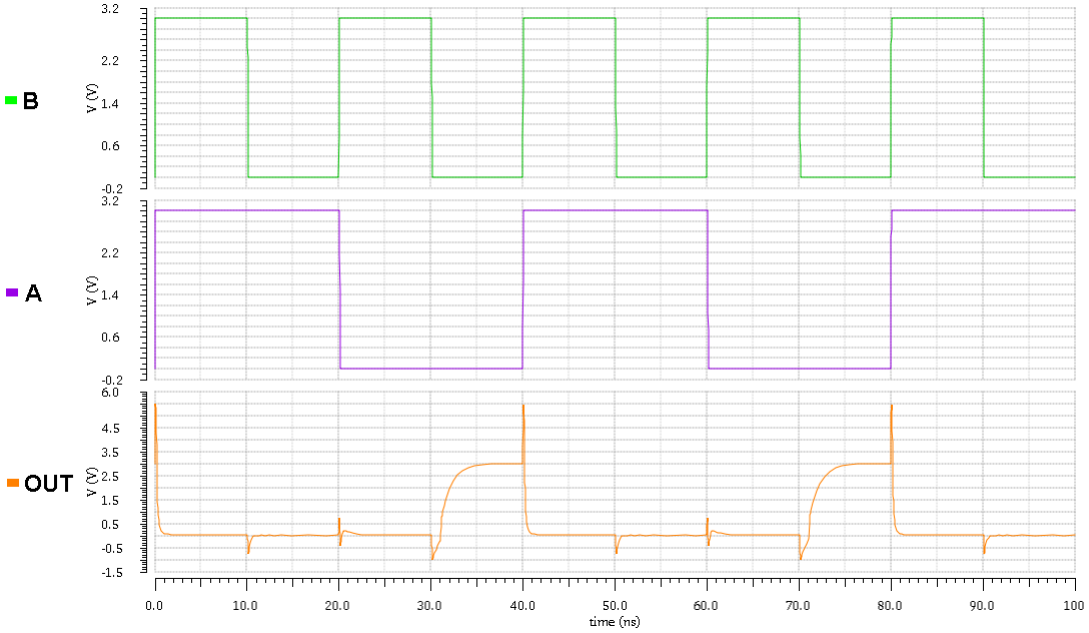


Figure 1.12: NOR gate schematic simulation results.

Figure 13 shows the NOR gate layout design. Note that this gate layout is larger and only used once, in the XNOR gate.

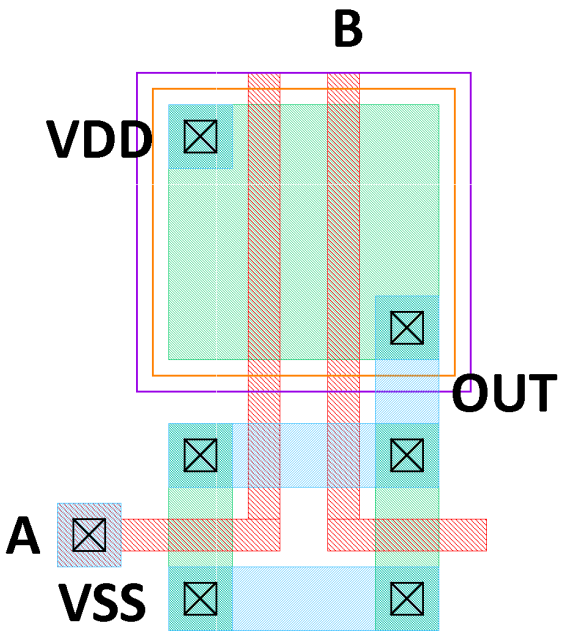


Figure 1.13: NAND gate layout design.

3.4 XNOR Gate

XNOR Gates will only output high if both inputs are equal. This gate also requires a reset that will output low when the reset is high. Table 5 shows the expected output from all possible inputs.

Table 5: NOR Gate truth table.

RST	A	B	OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 1.14 shows the XNOR gate schematic design. It incorporates four NAND gates and a NOR gate for the reset.

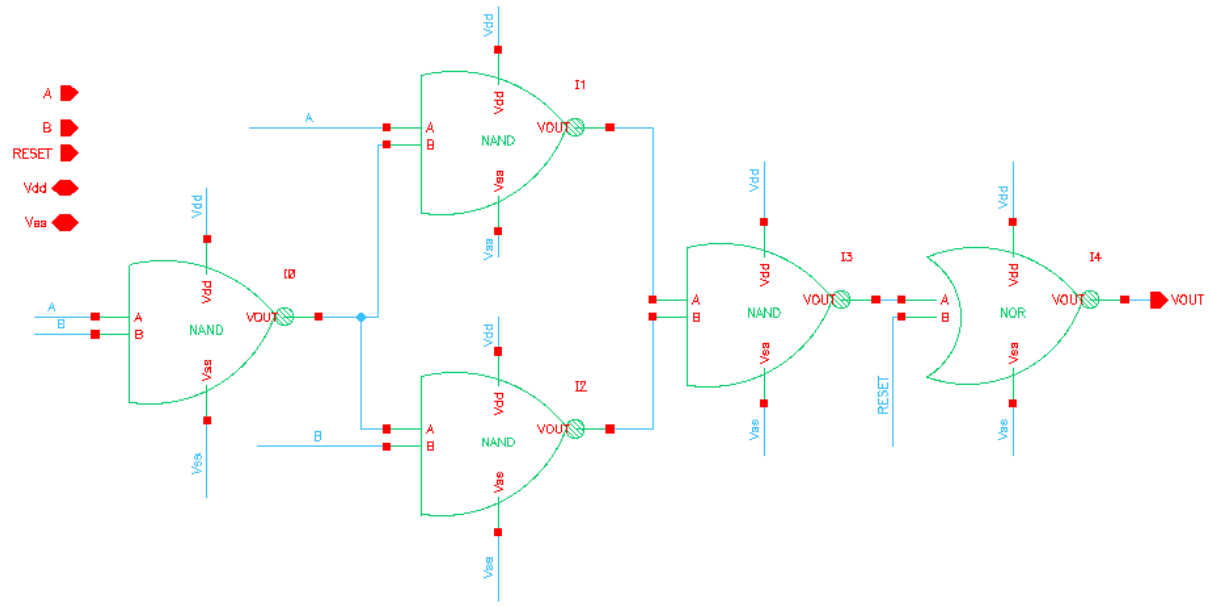


Figure 1.14: XNOR Gate schematic design.

Figure 1.15 shows the simulation results of the XNOR gate schematic. These results are found to be successful. The pull-down time is 11ns and the pull-up time is 12ns. Before the pull-up signal stabilises, the voltage peaks to well above the input values.

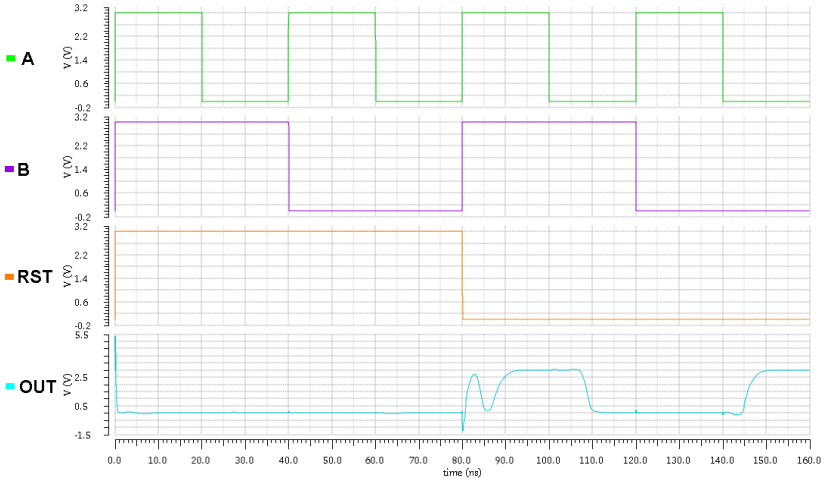


Figure 1.15: XNOR Gate schematic simulation results.

Figure 1.16 shows the XNOR gate layout design. The XNOR gate is the largest, and in this example, is even larger than the D Flip Flop. The size is not optimised because there was enough space to include it as is. However, given more time, this design could be made smaller.

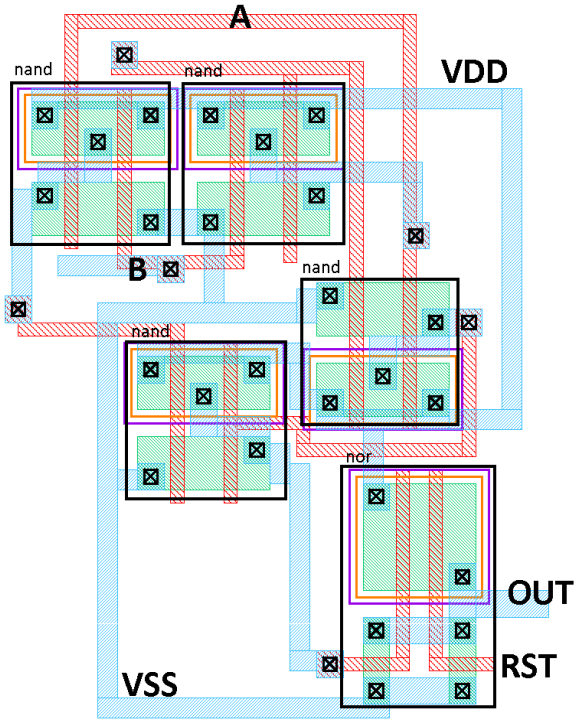


Figure 1.16: XNOR Gate layout design.

3.7 Master Clock Generator

The master clock generator (oscillator) will generate the clock from an external capacitor connected across both C1 and C2 pads in the circuit. Figure 1.17 shows the master clock generator schematic design. The circuit uses four inverters and an nmos with a length of 84u and a width of 4.8u.

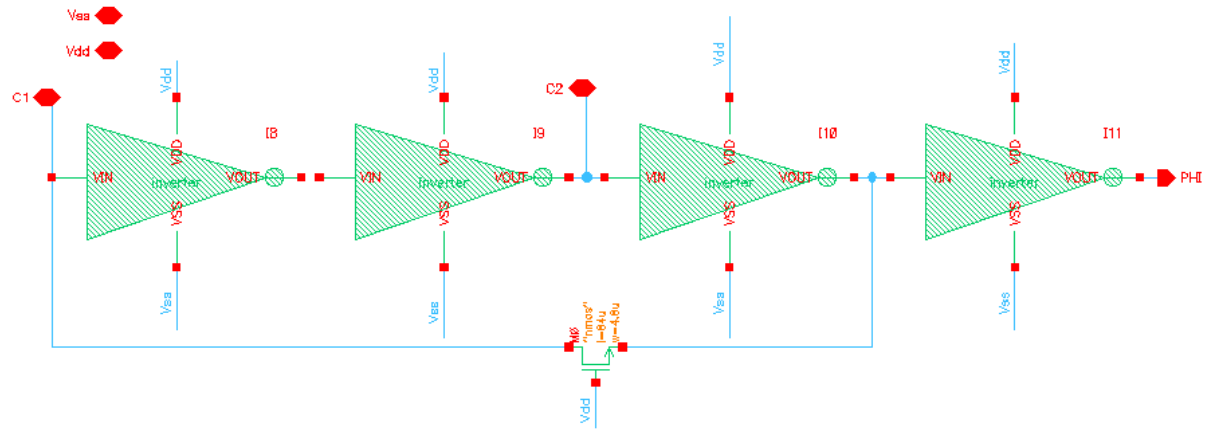


Figure 1.17: Master clock generator schematic design.

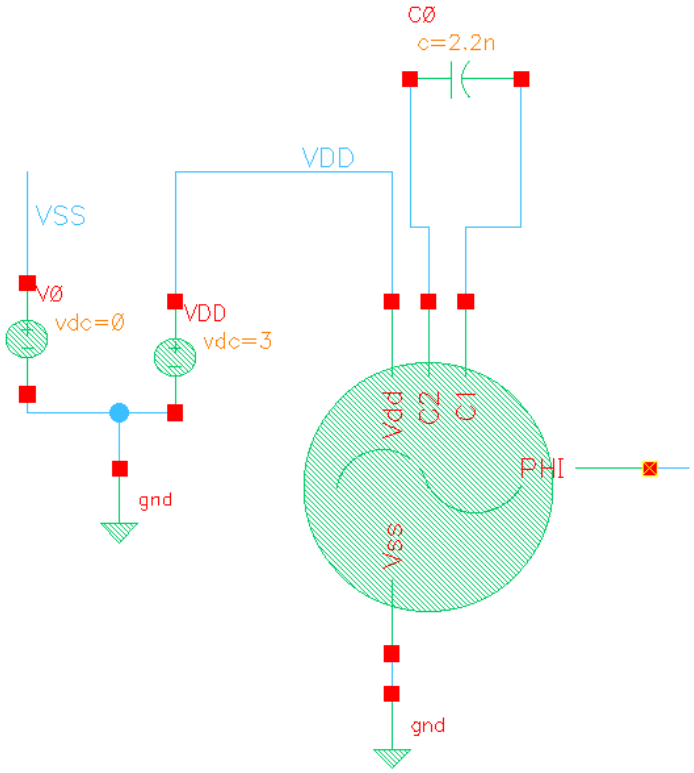


Figure 1.18: Testbench schematic design.

Figure 1.19 shows the simulation results of the master clock generator schematic. These results are found to be successful. The rise and fall times appear to be instantaneous.

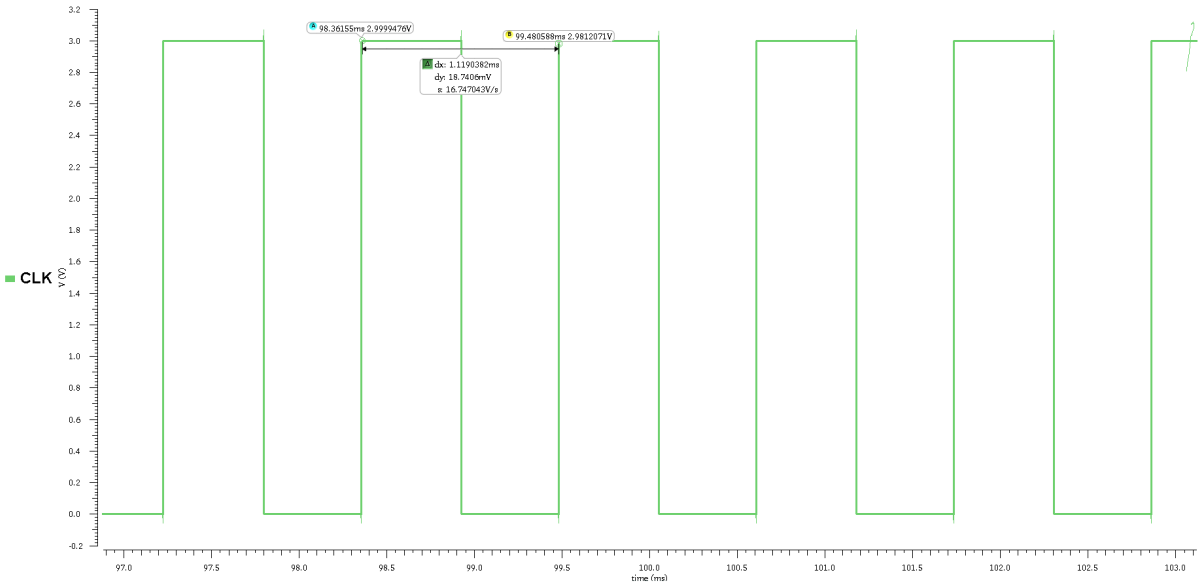


Figure 1.19: Master clock generator schematic simulation results.

Figure 1.20 shows the master clock generator layout design.

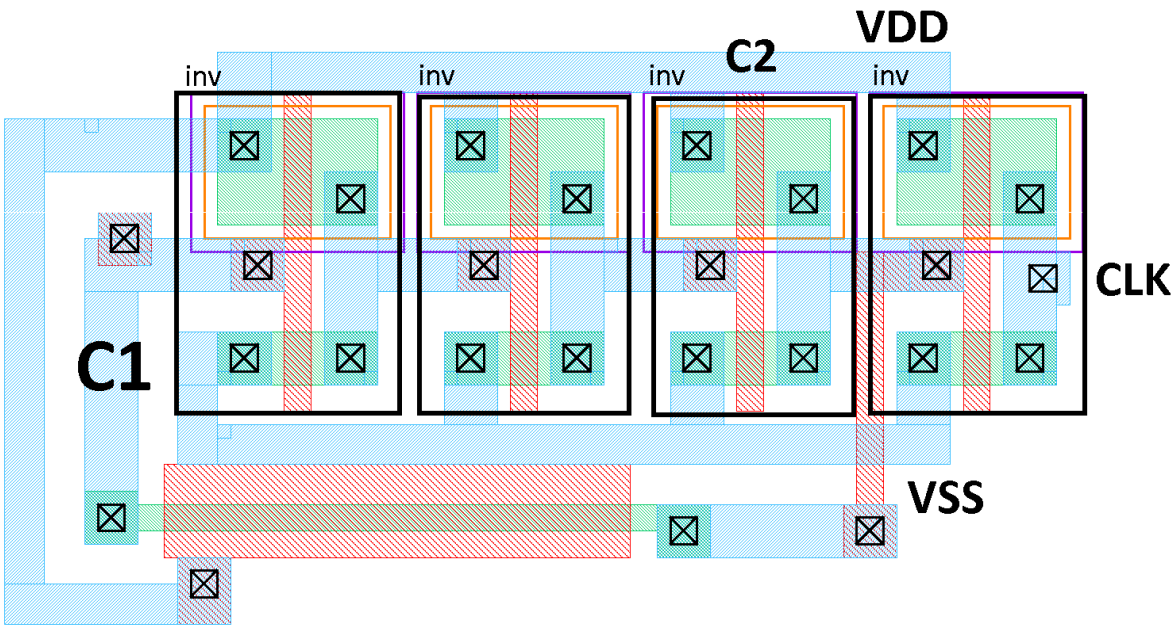


Figure 1.20: Master clock generator layout design.

3.6 D Flip-Flop

The D Flip Flop is a register that will hold the input from the rising edge of the clock. Figure 1.21 shows the D flip flop schematic design. The circuit incorporates two latches which each have four NAND gates and one inverter.

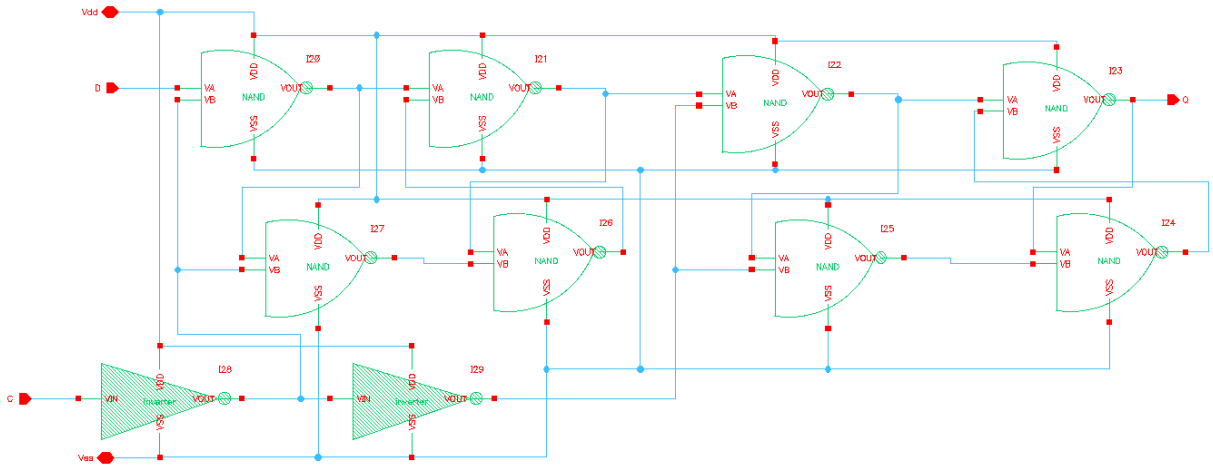


Figure 1.21: D Flip Flop schematic design.

Figure 1.22 shows the simulation results of theD flip flop schematic. These results are found to be successful. The pull-up and pull-down both take 20ns to stabilise.

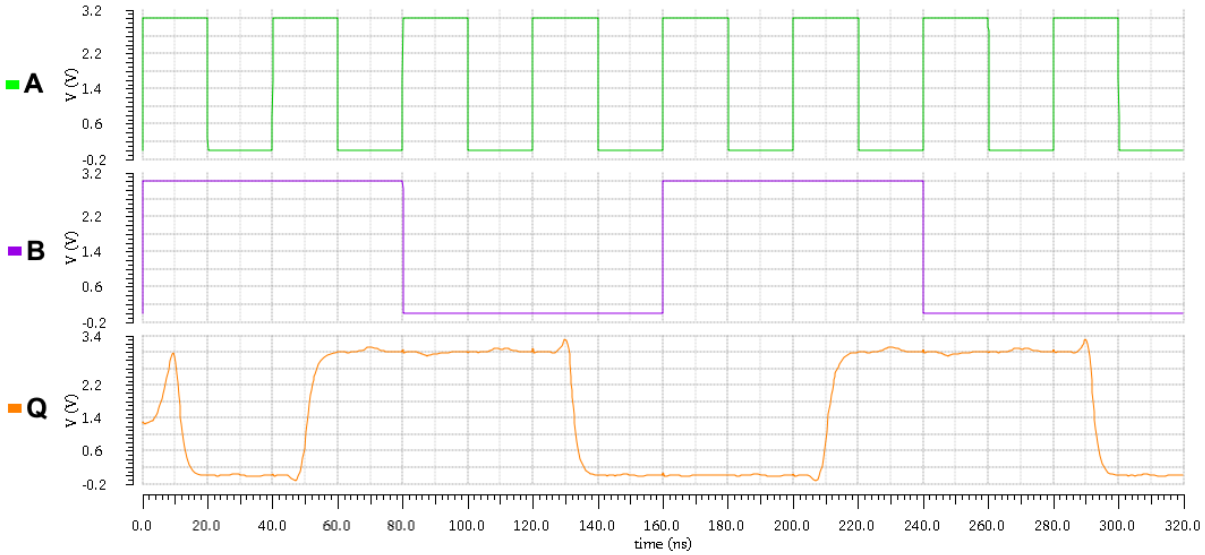


Figure 1.22: D Flip Flop schematic simulation results.

Figure 1.23 shows the D flip flop layout design. This layout was made as small as possible because five of them were required in the final design. The inverters were stretched along the side so that the flip flops could be stacked without wasting space. A vertical configuration was used so that three could fit together within 240λ (the maximum height of the chip).

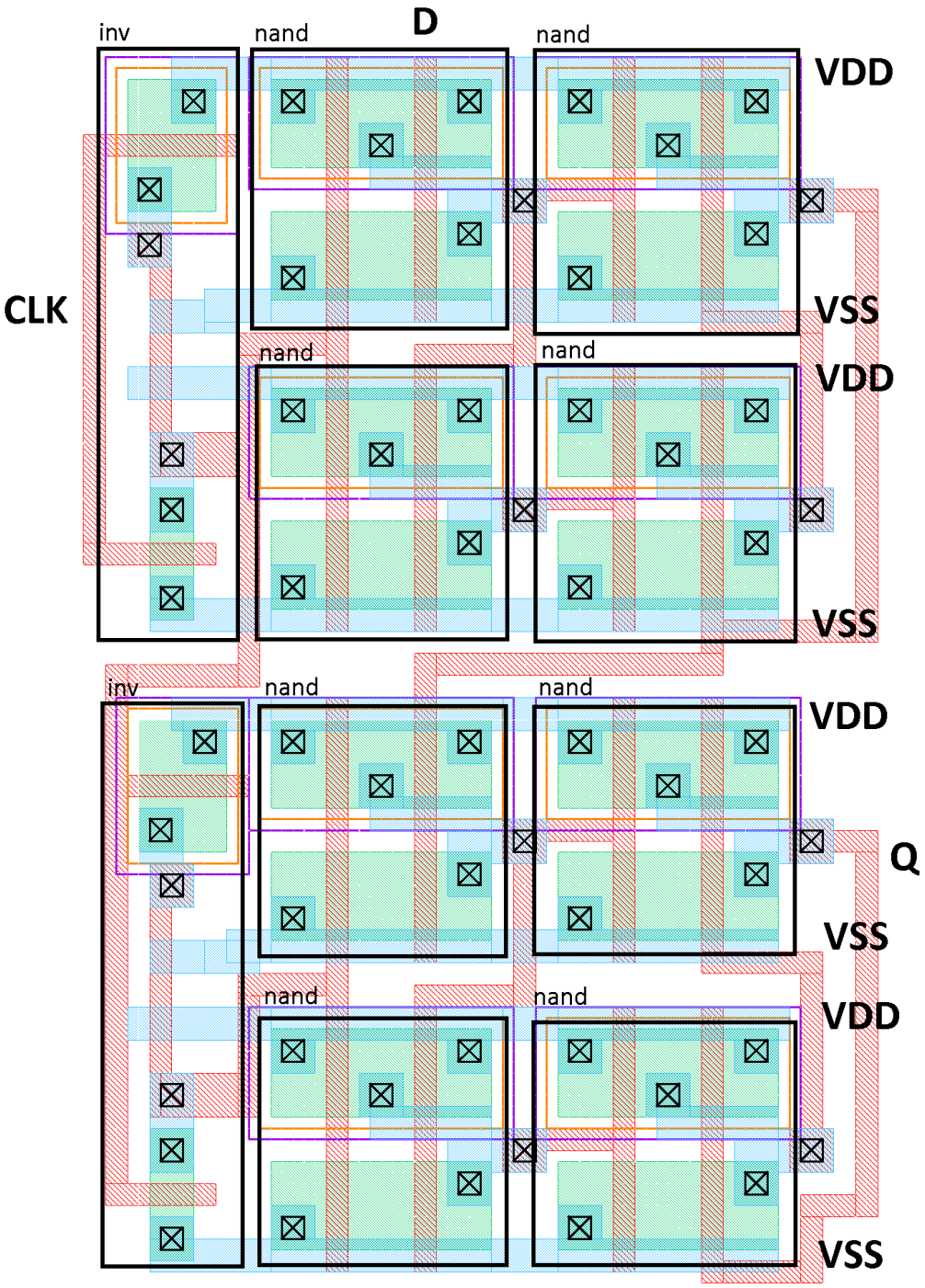


Figure 1.23: D Flip Flop layout design.

3.7 Output Driver

The output driver will be able to single 10mA of current. The output driver consists of a single wide nmos in open drain configuration connected to the VOUT minipad. An LED is also connected to it. The output driver schematic is shown in figure 1.24.

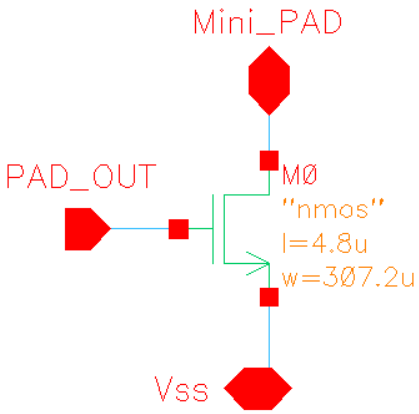


Figure 1.24: Output driver schematic design.

Figure 1.25 shows the simulation results of the output driver schematic.

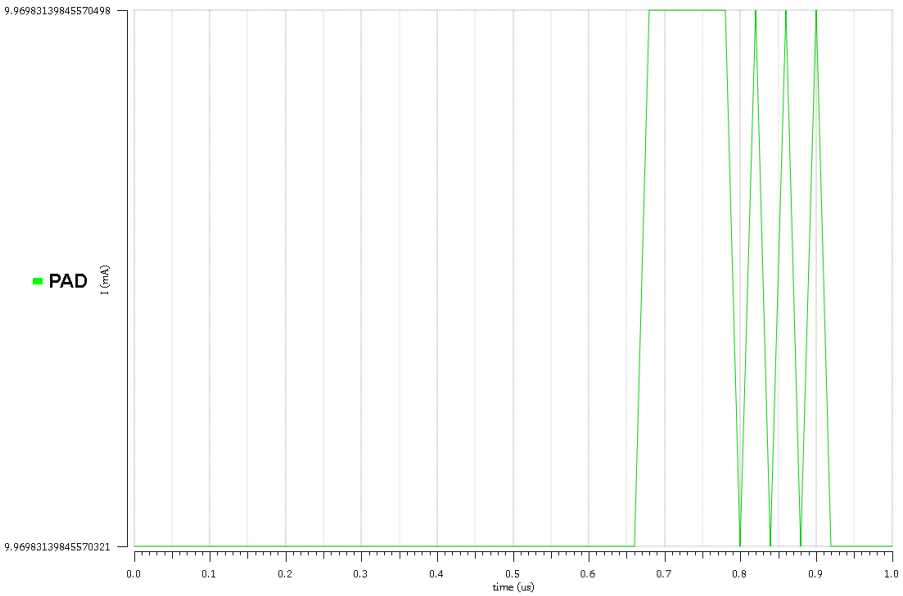


Figure 1.25: Output driver schematic simulation.

Figure 1.26 shows the output driver layout design. This layout uses as many nodes as possible in order to maintain signal integrity.

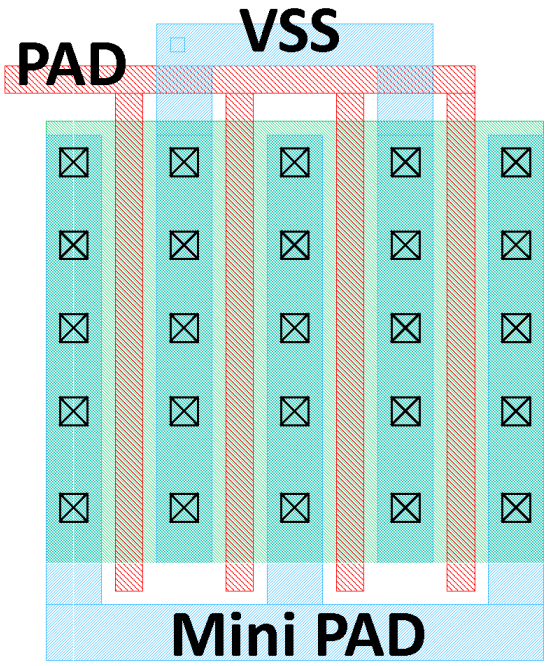


Figure 1.26: Output driver layout design.

4.0 HIGH LEVEL DISCUSSION

4.1 Input Protection

The input protection is meant to protect from 1kV for 1ns. The input protection should not allow more than 50V to pass through. This means that the input protection should have a high resistance. Trial and error was used to find the width of the nmos. The length is 4.8u and the width is 180u. The input protection schematic design is shown in figure 1.27.

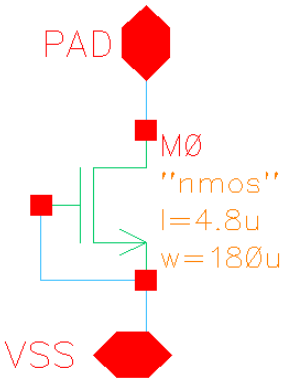


Figure 1.27: Input protection schematic design.

Figure 1.28 shows the simulation results for the input protection schematic. These results are found to be successful. The maximum voltage is under 50V.

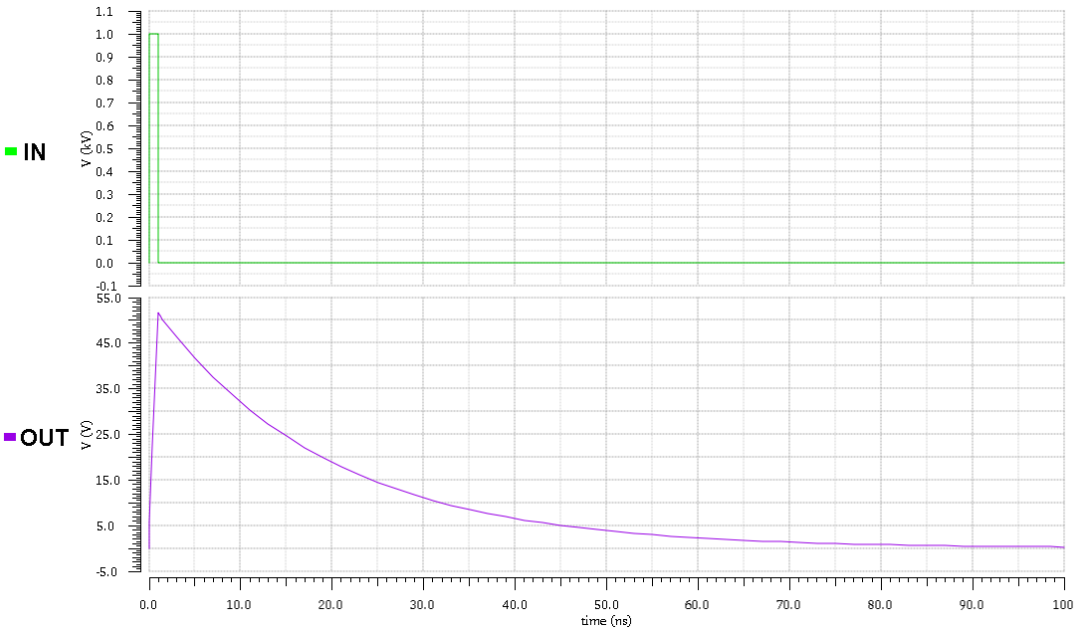


Figure 1.28: Input protection schematic simulation results.

Figure 1.29 shows the input protection layout design. This layout uses one long finger rather than multiple shorter fingers, because one finger increases the resistance of the transmission. The d-well material is used because it has the highest resistance.

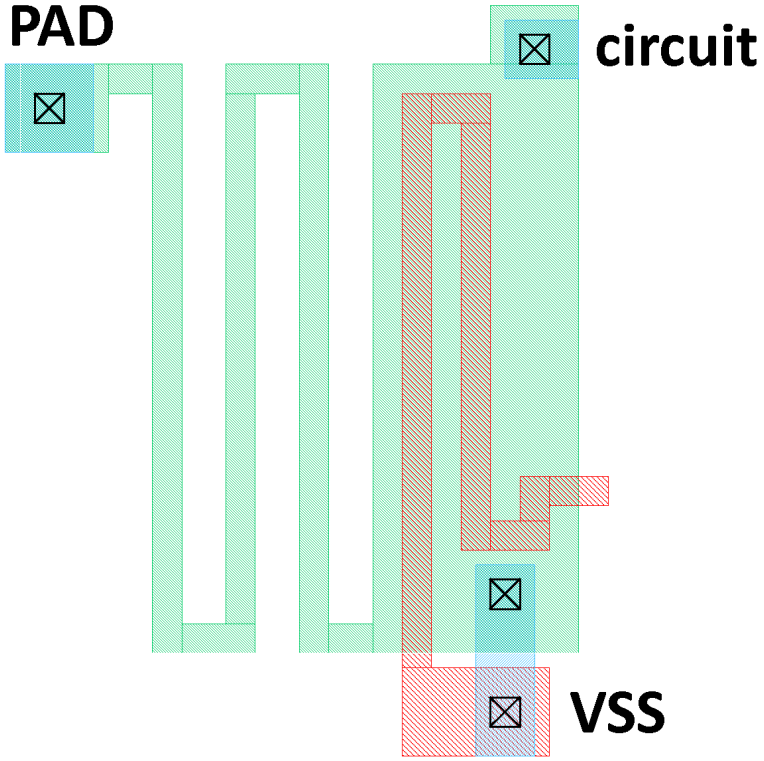


Figure 1.29: Input protection layout design.

4.2 PRSG

Figure 1.30 shows the complete PRSG schematic design. The design incorporates five D flip flops and one XNOR gate.

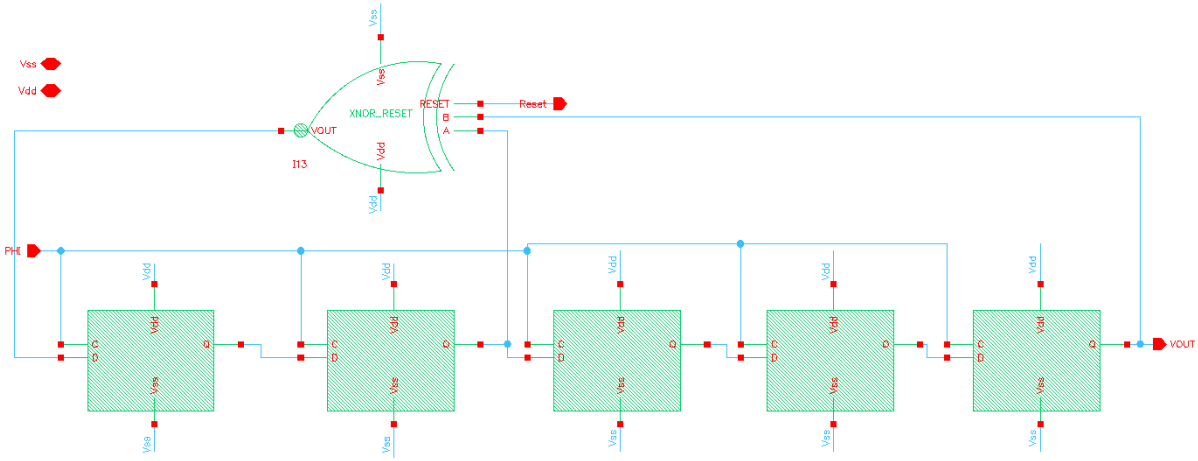


Figure 1.30: PRSG schematic design.

Figure 1.31 shows two full cycles of the simulation results for the PRSG. These results are found to be successful

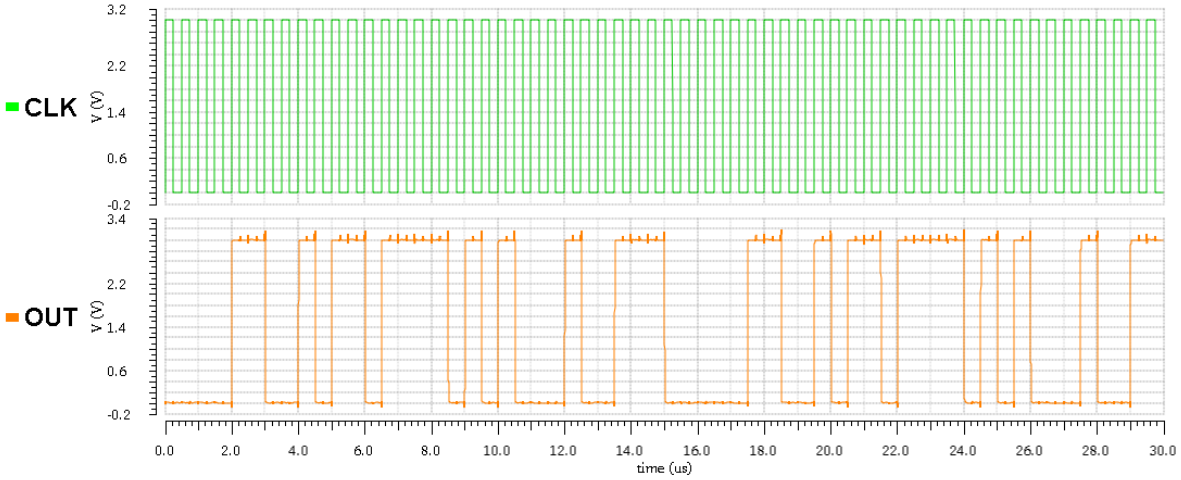


Figure 1.31: PRSG schematic simulation results.

Figure 1.32 shows the simulation results for the reset on the PRSG. The reset takes 3us to fully reset. These results are found to be successful

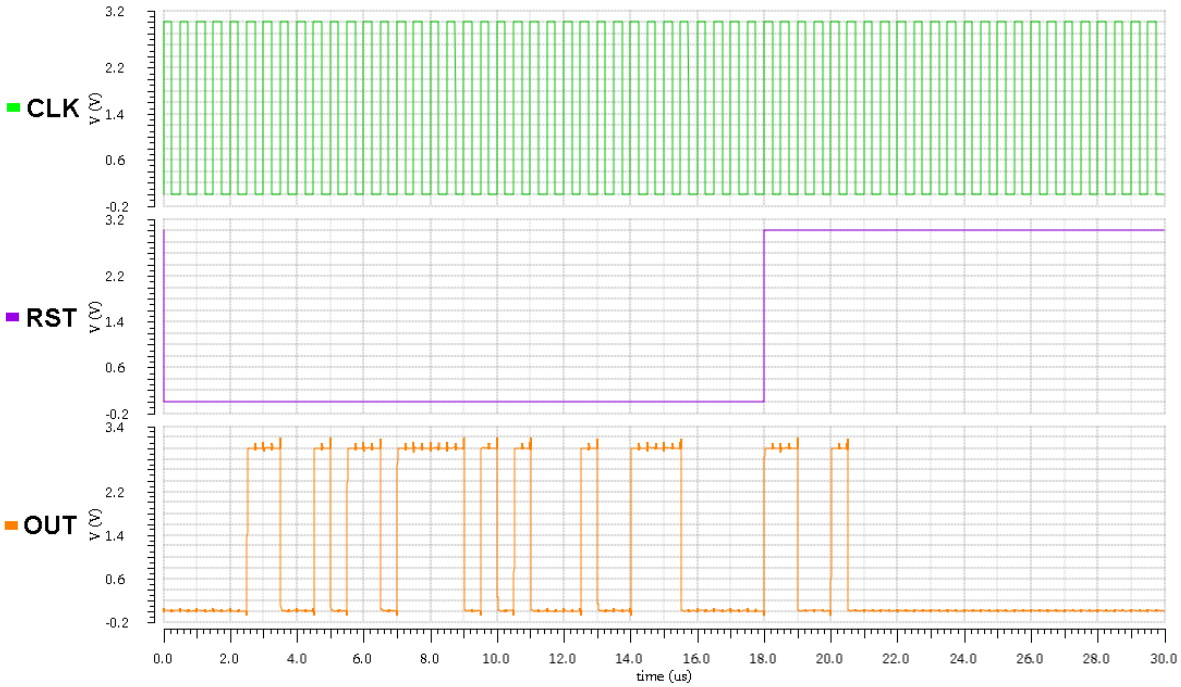


Figure 1.32: PRSG schematic simulation results with reset.

4.3 Top Level

Figure 1.33 shows the top level schematic design of the chip. The circuit incorporates inputs protections of each of the input pads (C1, C2, VIN, VDD) and an output driver on the output pad (VOUT).

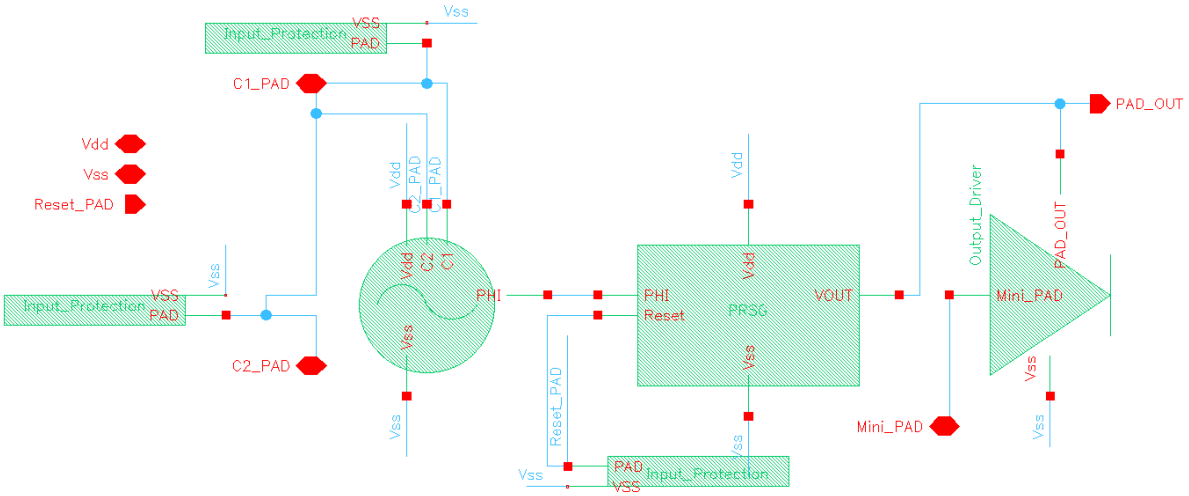


Figure 1.33: Top level schematic with all components.

Figure 1.34 shows the top level layout design of the chip.

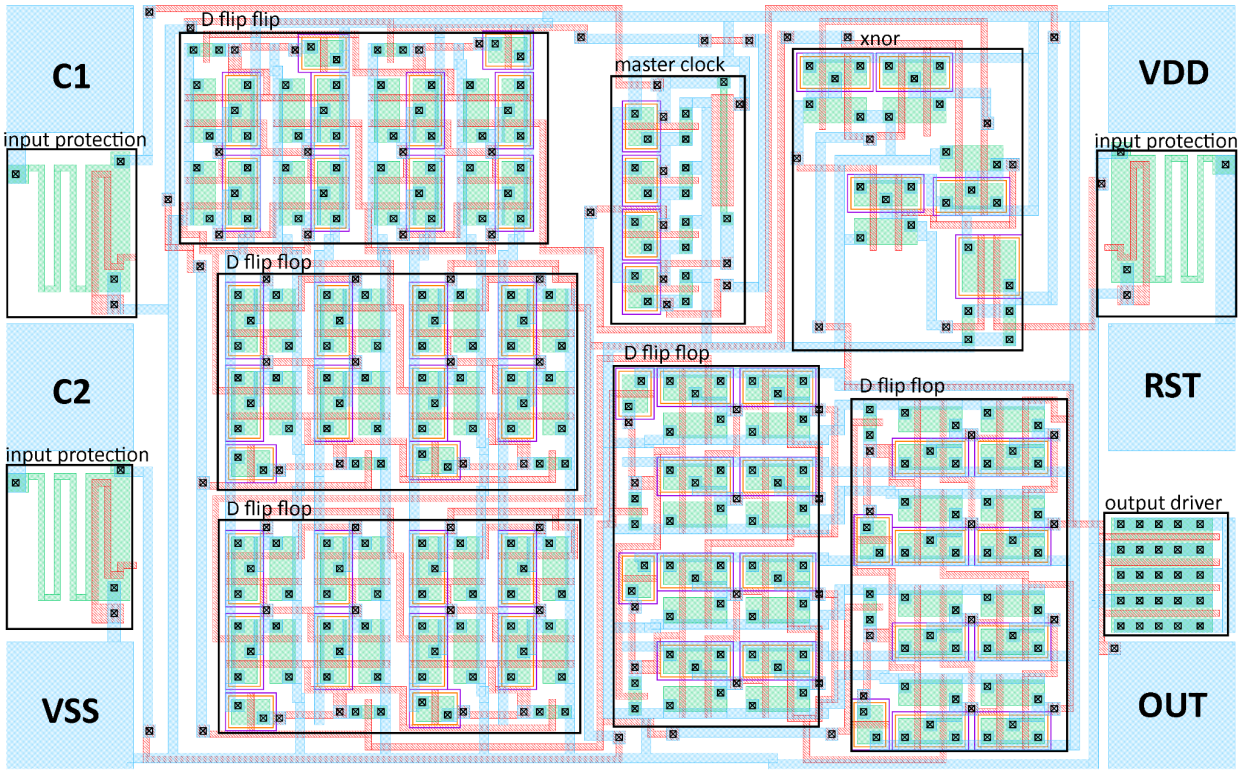


Figure 1.34: Top level layout design.

Figures 1.35 and 1.36 show that the layout passes LVS and DRC through due to both LVS happy face and drc.summary.

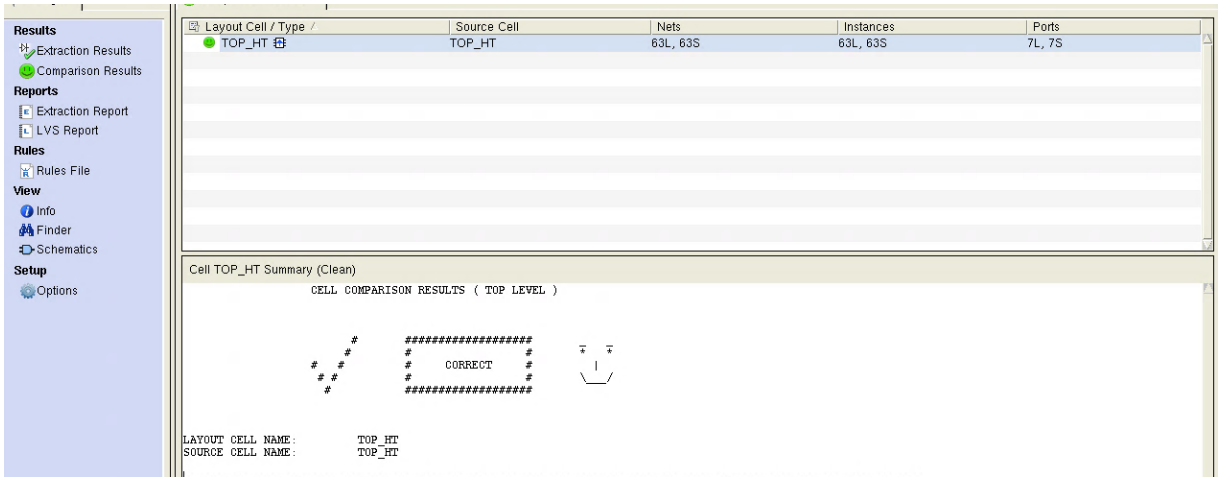


Figure 1.35: LVS pass confirmation.

```
--- RULECHECK RESULTS STATISTICS
---
RULECHECK METAL_WIDTH ..................... TOTAL Result Count = 0 (0)
RULECHECK METAL_SPACING ................... TOTAL Result Count = 0 (0)
RULECHECK POLY_WIDTH ...................... TOTAL Result Count = 0 (0)
RULECHECK POLY_SPACING .................... TOTAL Result Count = 0 (0)
RULECHECK FIELD_POLY_DWELL_SPACING ........ TOTAL Result Count = 0 (0)
RULECHECK FIELD_POLY_SOURCE_DRAIN_TOUCHING ... TOTAL Result Count = 0 (0)
RULECHECK DWELL_WIDTH ..................... TOTAL Result Count = 0 (0)
RULECHECK DWELL_SPACING ................... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_WIDTH ................... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_METAL_OVERLAP ........... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_POLY_OVERLAP ............ TOTAL Result Count = 0 (0)
RULECHECK CHANNEL_CONTACT_SPACING ......... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_D_WELL_OVERLAP .......... TOTAL Result Count = 0 (0)
RULECHECK NWELL_DWELL_OVERLAP.1 ........... TOTAL Result Count = 0 (0)
RULECHECK NWELL_DWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_NWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_P_SOURCE_DRAIN_ENCLOSURE .. TOTAL Result Count = 0 (0)
RULECHECK Pplus_DWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_N_SOURCE_DRAIN_SPACING .... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK Grid.1 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.2 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.3 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.4 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.5 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.6 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.7 .......................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_METAL .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_POLY ..................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_DWELL .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_NPLUS .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_PPLUS .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_CONTACT .................. TOTAL Result Count = 0 (0)
RULECHECK ART_TO_NWELL .................... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                 0
TOTAL REAL Time:                0
TOTAL Original Layer Geometries: 747 (2145)
TOTAL DRC RuleChecks Executed:  36
TOTAL DRC Results Generated:    0 (0)
```

Figure 1.36: DRC summary.

Chapter 2: IC Project Testing

1.0 INTRODUCTION

The testing is done using a Wentworth Probe Station and the waveforms are measured and recorded using an oscilloscope. Both fabrication and testing is done in the Carleton University Microelectronics Fabrication Facility. Figure 2.1 shows the probe station that was used with connection to the oscilloscope, capacitor, and input currents.

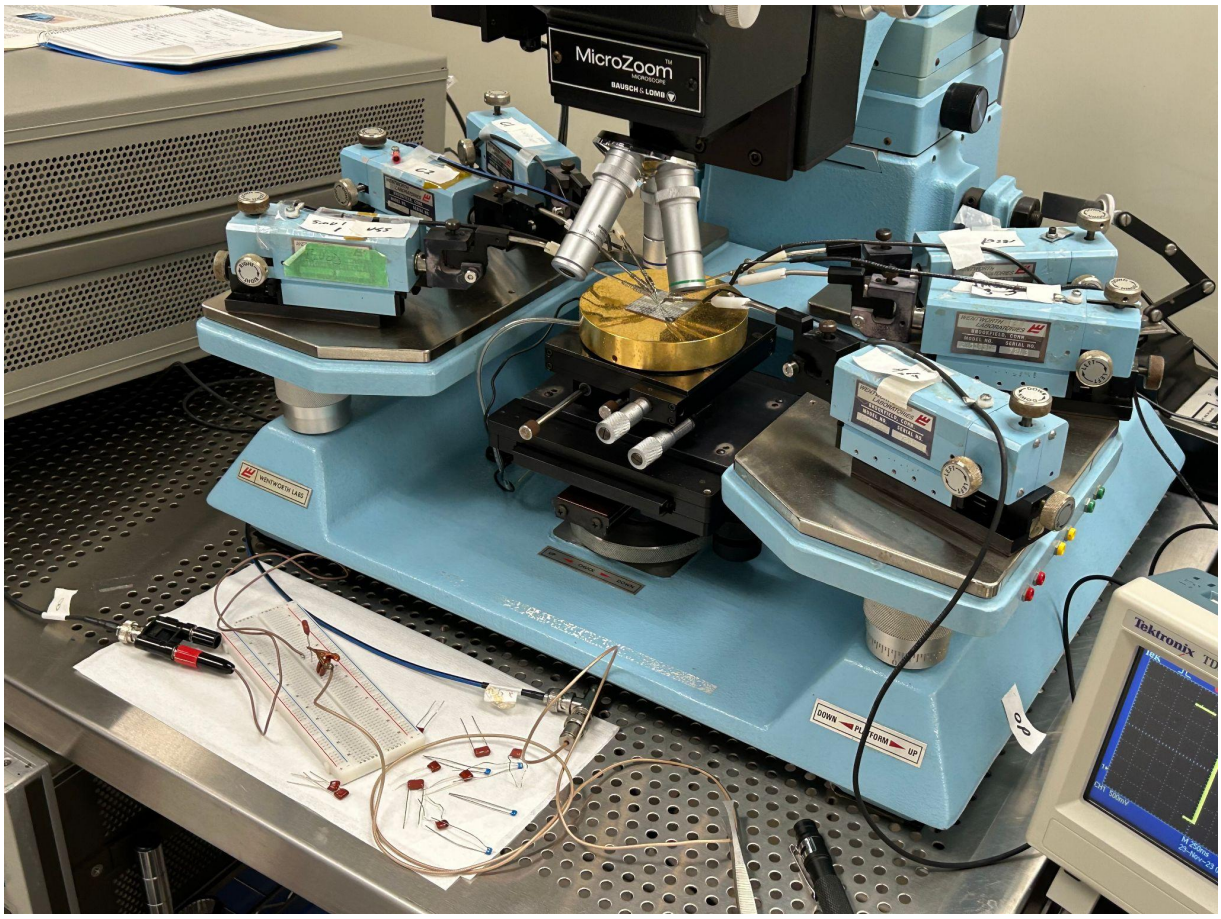


Figure 2.1: Photograph of chip in the Wentworth Probe Station at Carleton University.

Six probes connected to the pads of the chip. These are thin metal rods that are delicately moved to connect to the pads using Wentworth Probe Station. Figure 2.2 shows the probes connected to the pads.

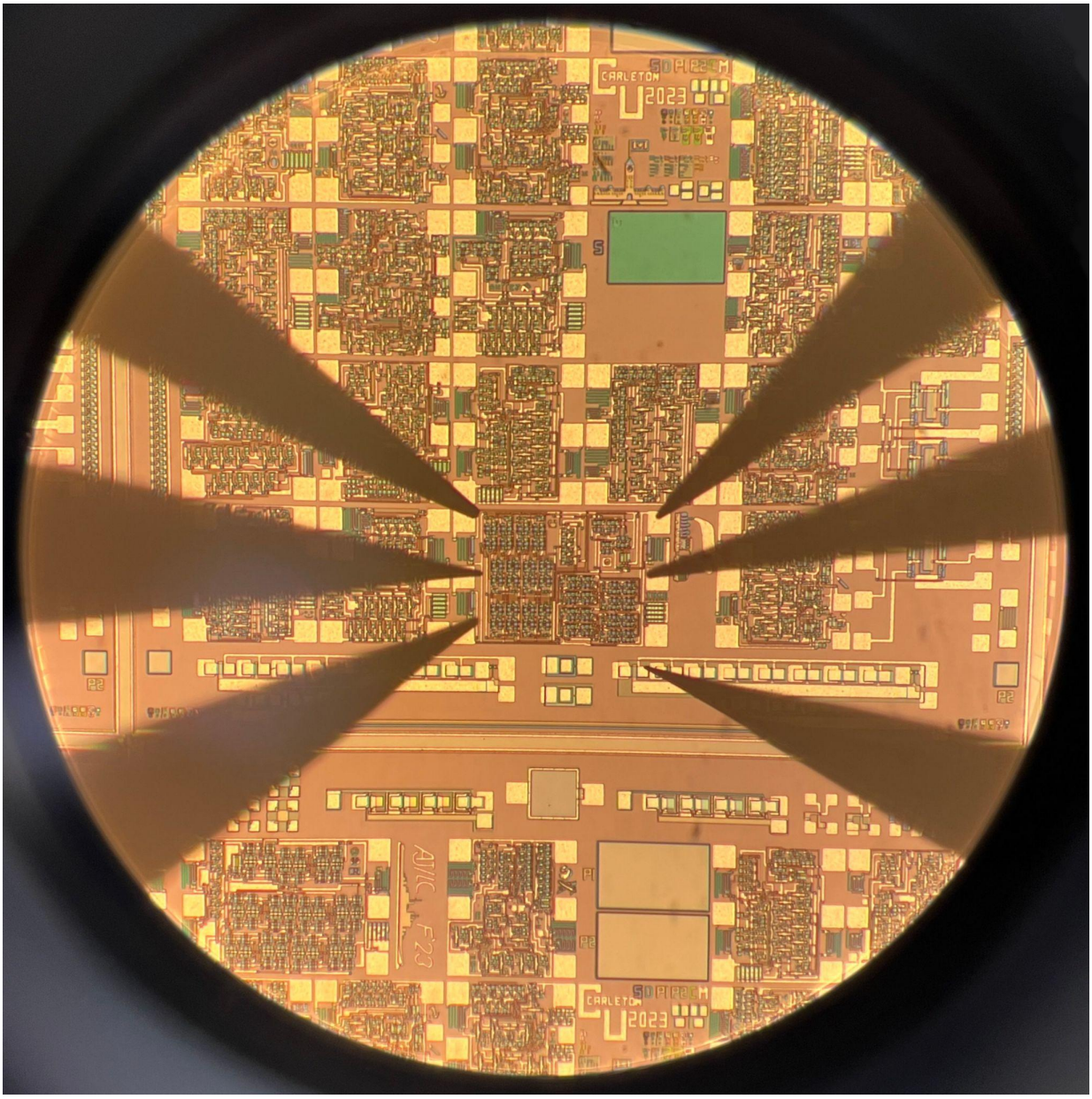


Figure 2.2: Photograph through microscope of probes connected to the pads.

A 10nF capacitor is connected between pads C1 and C2. It will provide a clock frequency near 1kHz to make testing simpler. A digital oscilloscope is connected to the VOUT pad. It can also be connected to the C2 pad to test the clock cycle. Finally, an HP 4155A Semiconductor Analyzer is connected to the RESET pad. Figure 2.3 shows the completed chip.

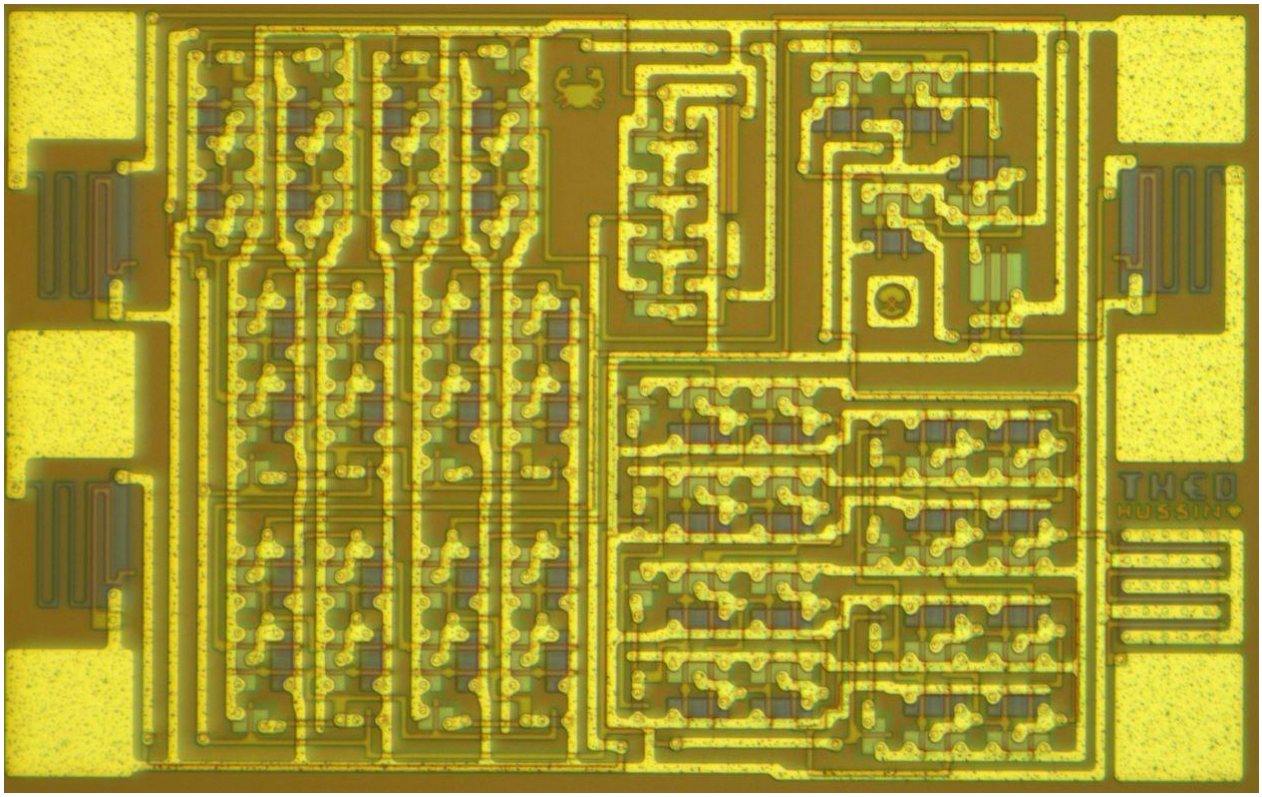


Figure 2.3: Photograph of completed chip.

Testing Equipment Used in Lab:

- HP 4155A Semiconductor Analyzer
- Wentworth Probe Station w/ 6 Probes (5 If you built a counter)
- TekTronix TDS2024C Digital Oscilloscope

1.1 Measured Results

Figure 2.4 shows the measured pseudorandom output waveform. These results are found to be unsuccessful because they do not match the expected pseudorandom sequence. After some time the output remains high.

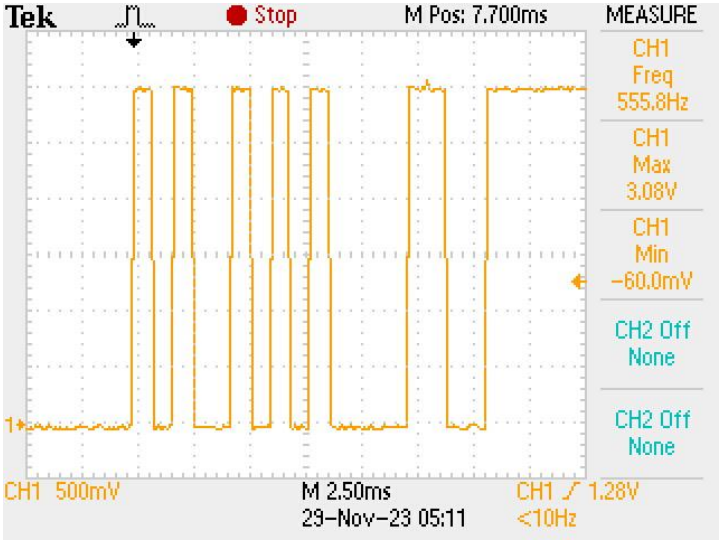


Figure 2.4: Measured pseudorandom output waveform.

Figure 2.5 shows the measured clock signal from the C2 pad as seen from the oscillator in the lab.

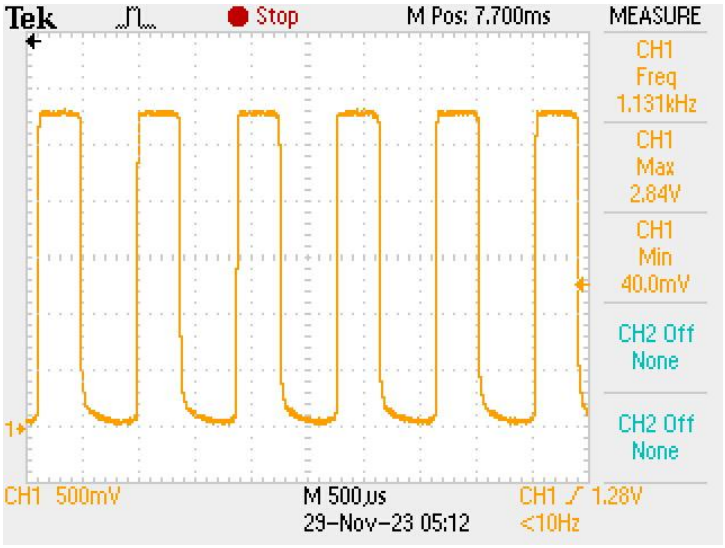


Figure 2.5: Measured clock signal at the C2 minipad.

2.0 TEST RESULTS

As shown in figure 2.6, these results are found to be successful. They are regular and consistent. The measured clock wavelength is 0.00531 - 0.006194 = 0.884 ms.

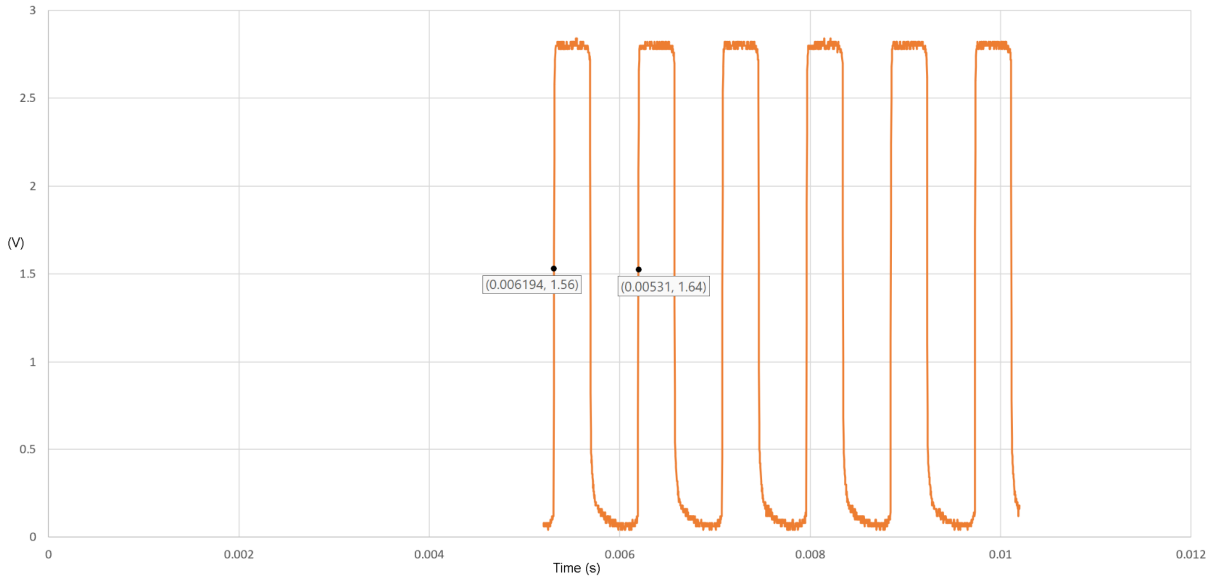


Figure 2.6: Measured clock signal at the C2 minipad.

As shown in figure 2.7, the expected clock wavelength is 1.11 ms. These values are close enough to count the master clock generators as successful. The reason the values are not exactly the same is because of the capacitor. Modifying the capacitor will allow for a more precise clock frequency.

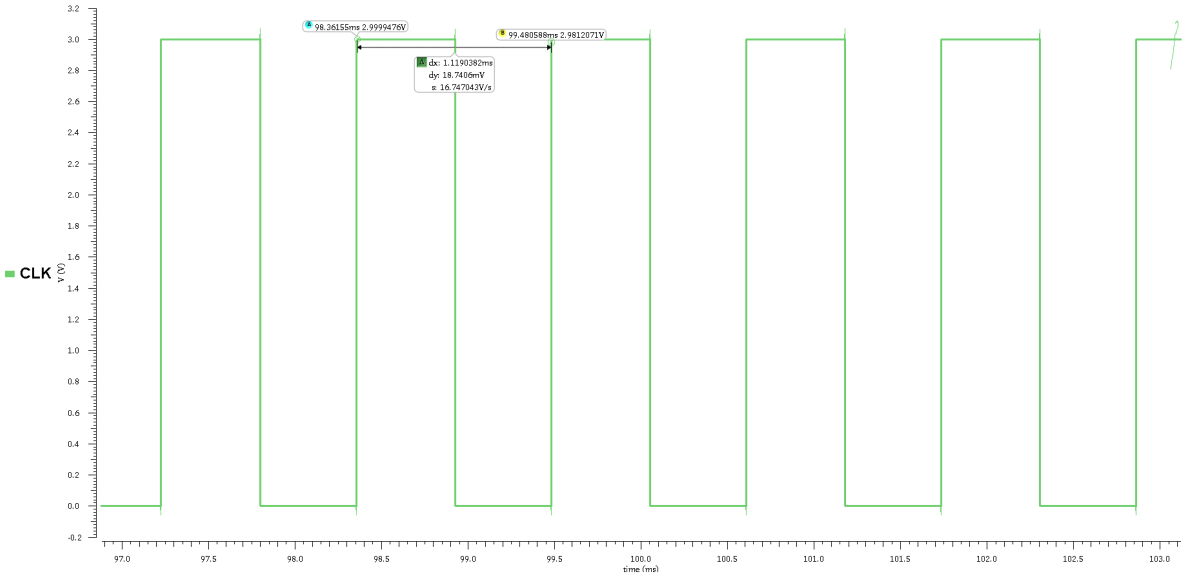


Figure 2.7: Expected clock signal at the C2 minipad.

Figure 2.8 shows the measured output waveform from the oscillator during testing. Figure 2.9 shows the expected output waveform.

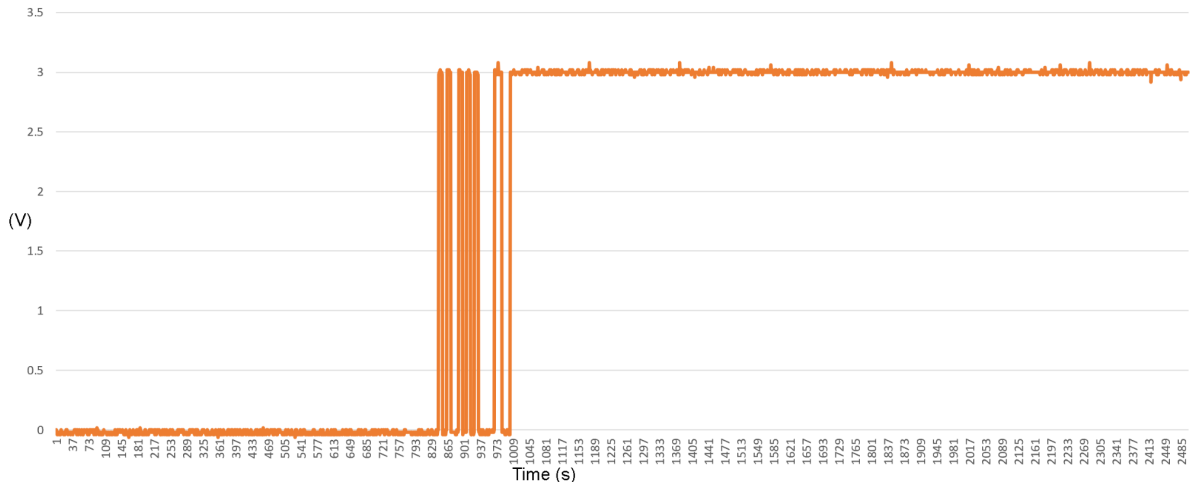


Figure 2.8: Measured pseudorandom output waveform.

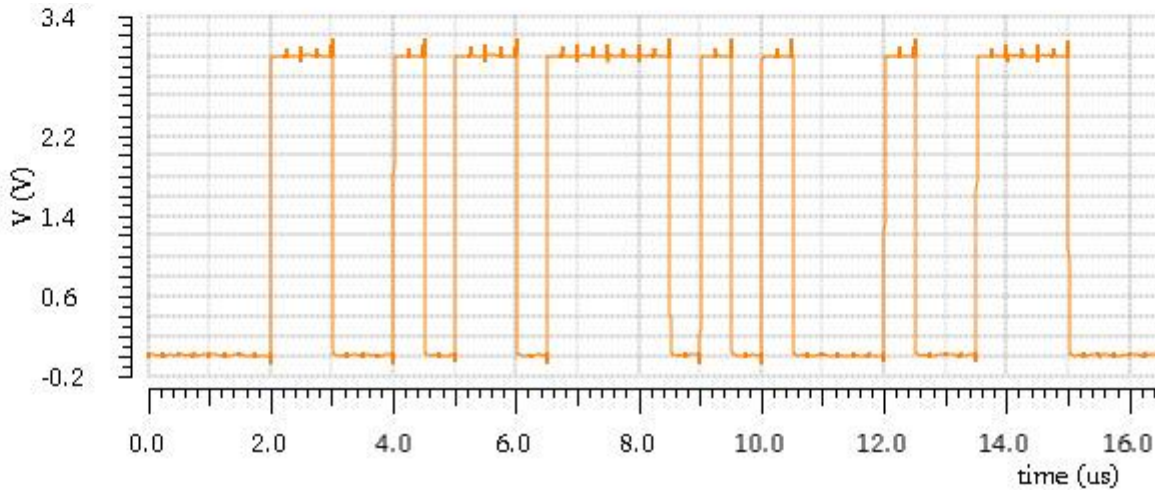


Figure 2.9: Expected pseudo-random output waveform.

As shown above the results of the measured Pseudo-random output does not match the expected value. Since both DRC and LVS passed, then the error could be caused by one or a combination of the following:

Voltage or current tolerances of individual components were exceeded, issues with power supply and delivery into the pseudo-random sequence generator, variations in temperature, software bug or logic errors, signal integrity issues and hardware malfunctions. These hardware malfunctions could be anything from poor connections, components failing and/or improper material for components or wires.

Chapter 3: Op-Amp Layout Project

1.0 INTRODUCTION

This project focuses on the design approach for a two-stage operational amplifier using a 45nm soi CMOS process. Operational-amplifiers are highly versatile components that can be utilised in many electronic systems. Initially students will begin by creating the given schematic in Cadence.
Figure 3.1 shows the Op-Amp design schematic.

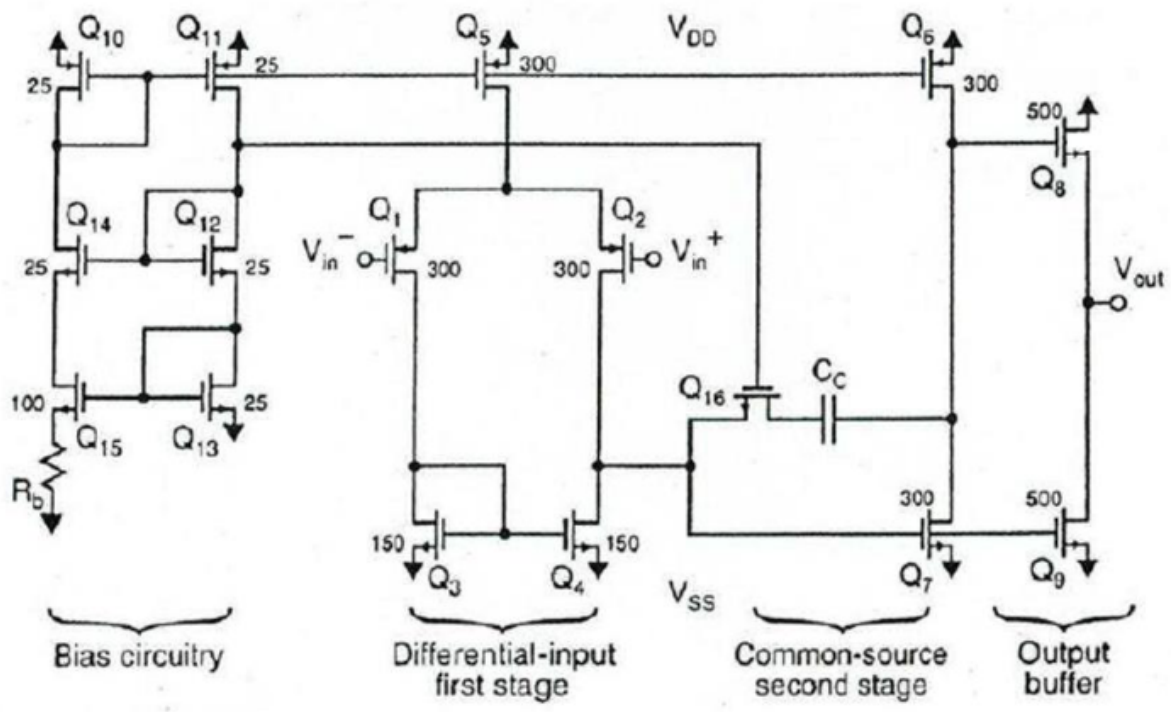


Figure 3.1: Op-Amp design schematic.

Using the schematic made in Cadence, we will initially simulate the operational amplifier under nominal conditions. Following this we will again simulate the schematic however varying the Processes, Voltages and Temperature. A total of 27 sets of data will be accrued. After getting a good understanding of the operational amplifier through the simulations, we design a top level layout floor plan based on the transistor dimensions that are provided below.

Table 6: Given transistor ratios and fingers.

Transistor	Type	(W/L)	Length (nm)	Width (um)	Fingers
Q1	P	300	40	12	6
Q2	P	300	40	12	6
Q3	N	150	40	6	3
Q4	N	150	40	6	3
Q5	P	300	40	12	6
Q6	P	300	40	12	6
Q7	N	300	40	12	6
Q8	N	2500	40	100	50
Q9	N	2500	40	100	50
Q10	P	25	40	1	1
Q11	P	25	40	1	1
Q12	N	25	40	1	1
Q13	N	25	40	1	1
Q14	N	25	40	1	1
Q15	N	100	40	4	2
Q17	N	25	40	1	1

Finally with the top level layout floor plan complete the final step is to create the layout view using the floorplan created. Extracting the layout view we will simulate the schematic vs extracted view for various cases.

2.0 SCHEMATIC SIMULATION

In cadence the schematic was created based on the given parameters. Following this the following results were obtained. Figures 3.2 and 3.3 show both the schematic design and testbench design.

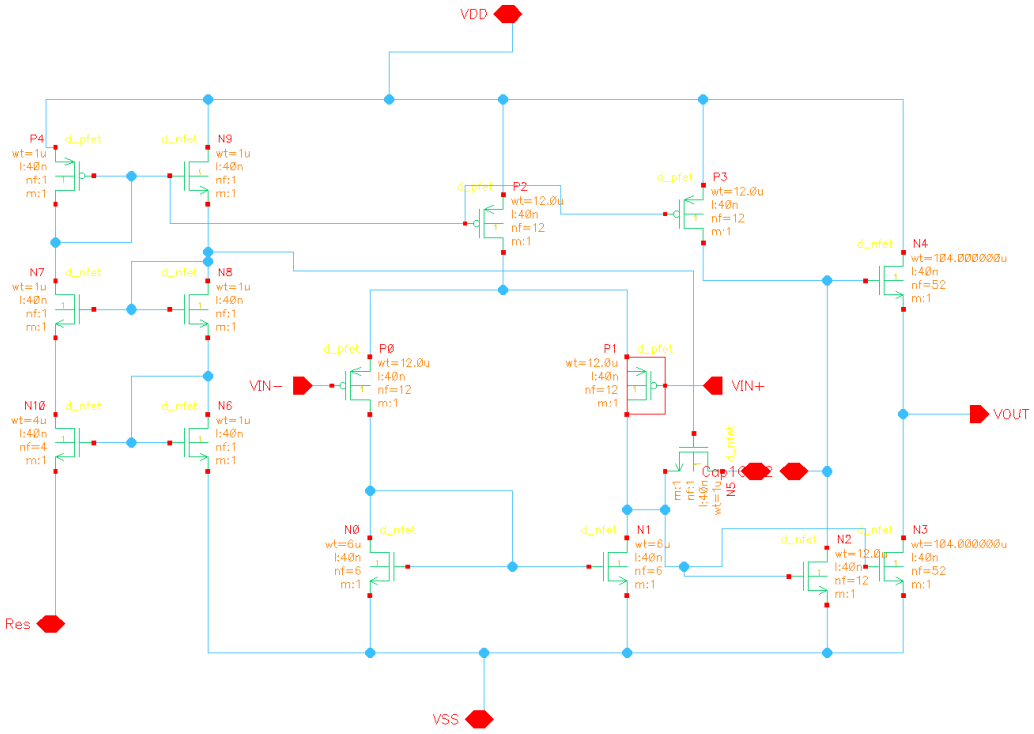


Figure 3.2: Operational Amplifier Schematic in Cadence.

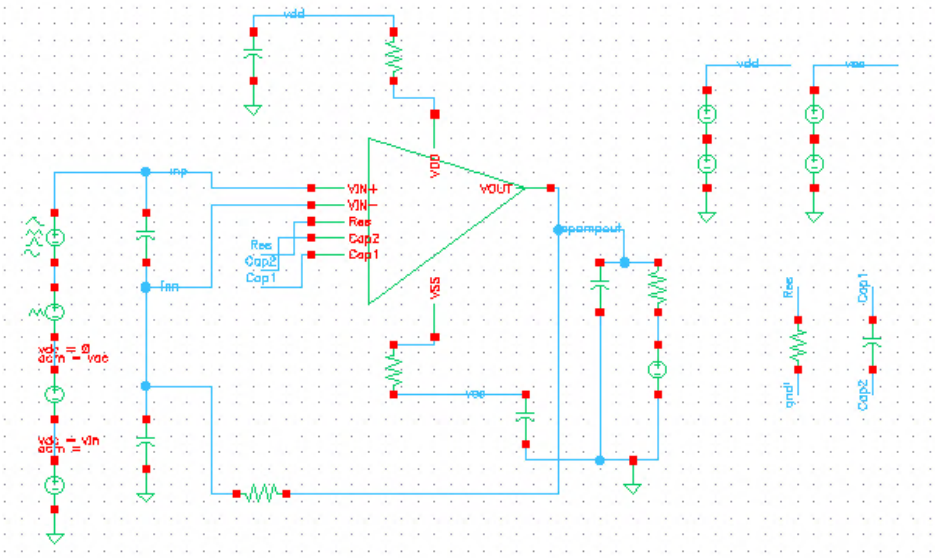


Figure 3.3: Testbench Operational Amplifier Schematic in Cadence.

Beginning with simulations under nominal conditions (NN, 1.2V, 25°C):

Open Loop Gain:
20.38

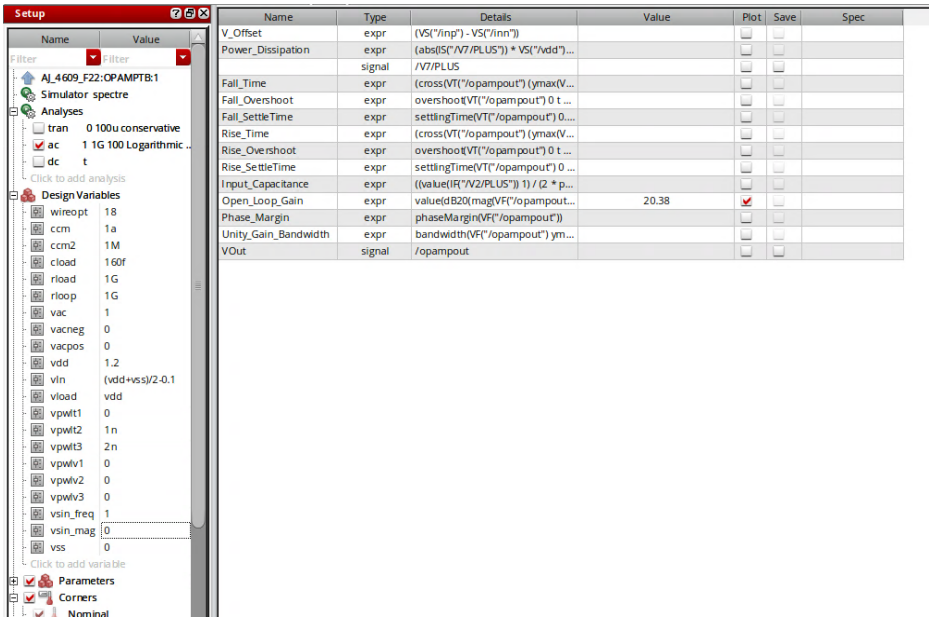


Figure 3.4: Open loop gain under normal conditions.

Unity Gain Bandwidth:
2.043MHz

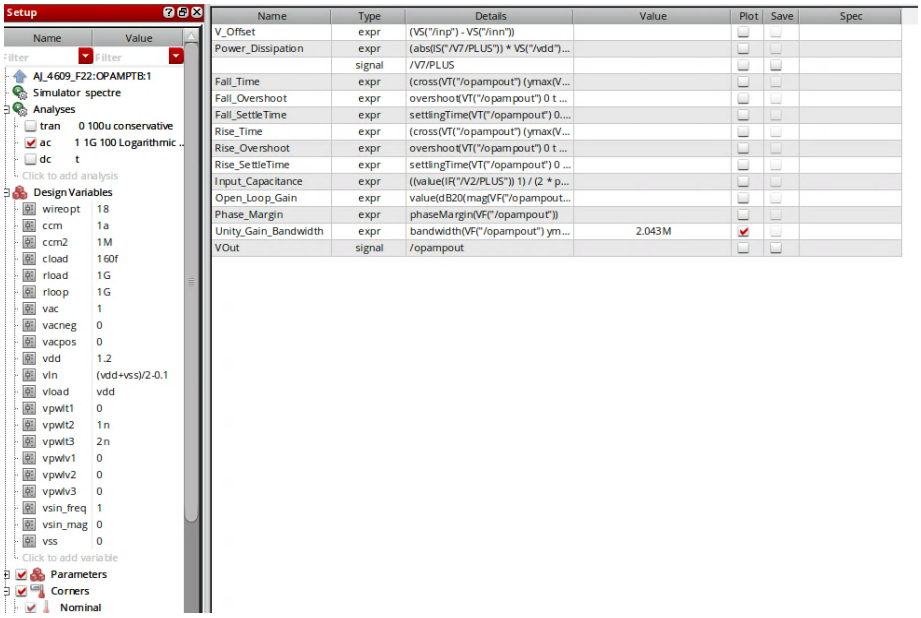


Figure 3.5: Unity gain bandwidth under normal conditions.

Phase Margin:

110.8°

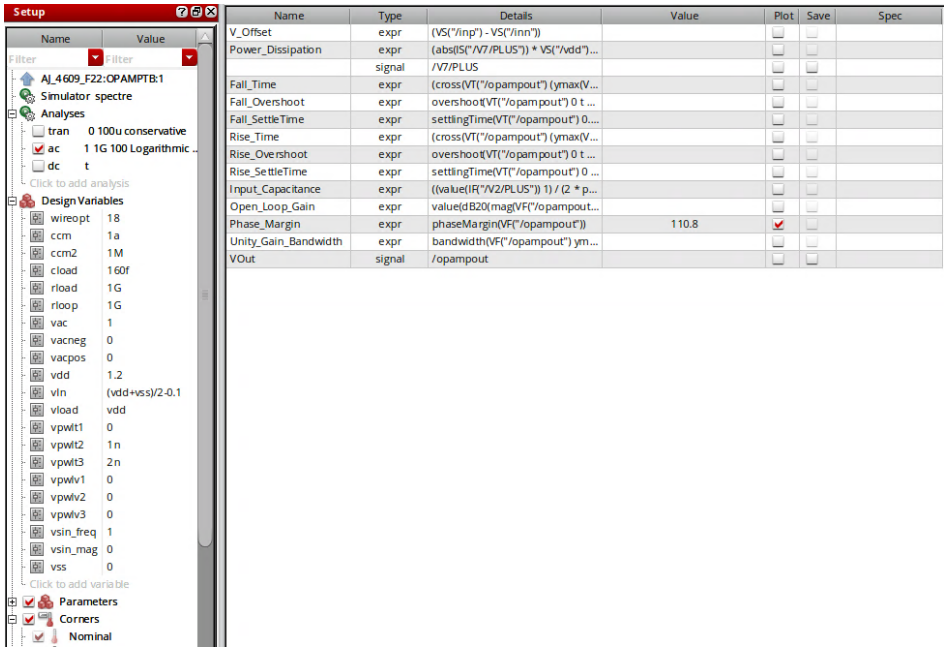


Figure 3.6: Phase margin under normal conditions.

Power Dissipation:

864.8uW

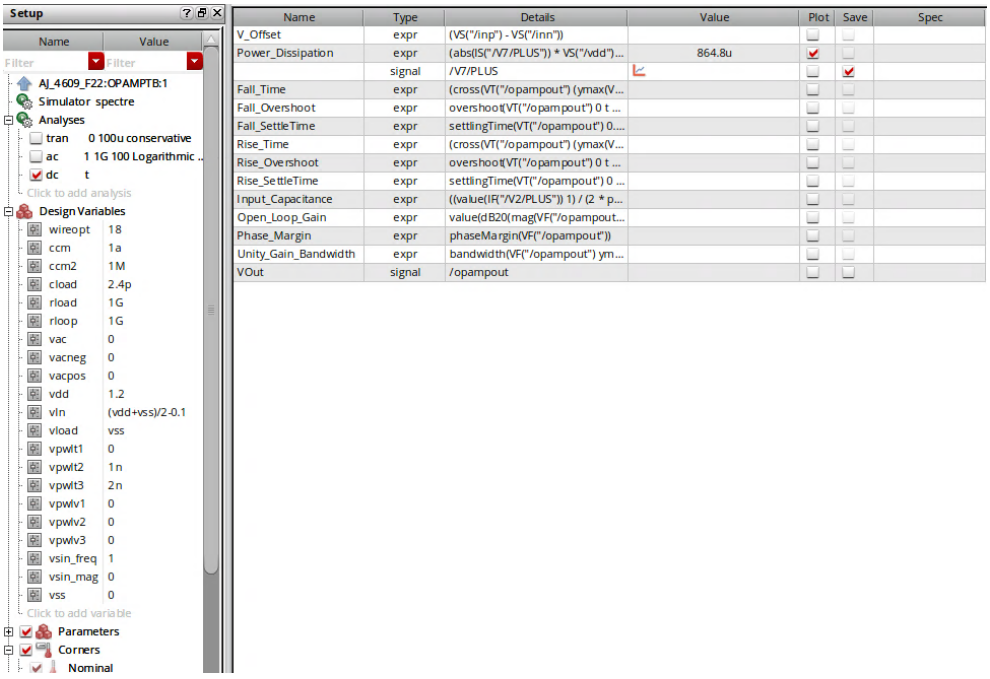


Figure 3.7: Power dissipation under normal conditions.

Voffset:
19.19mV

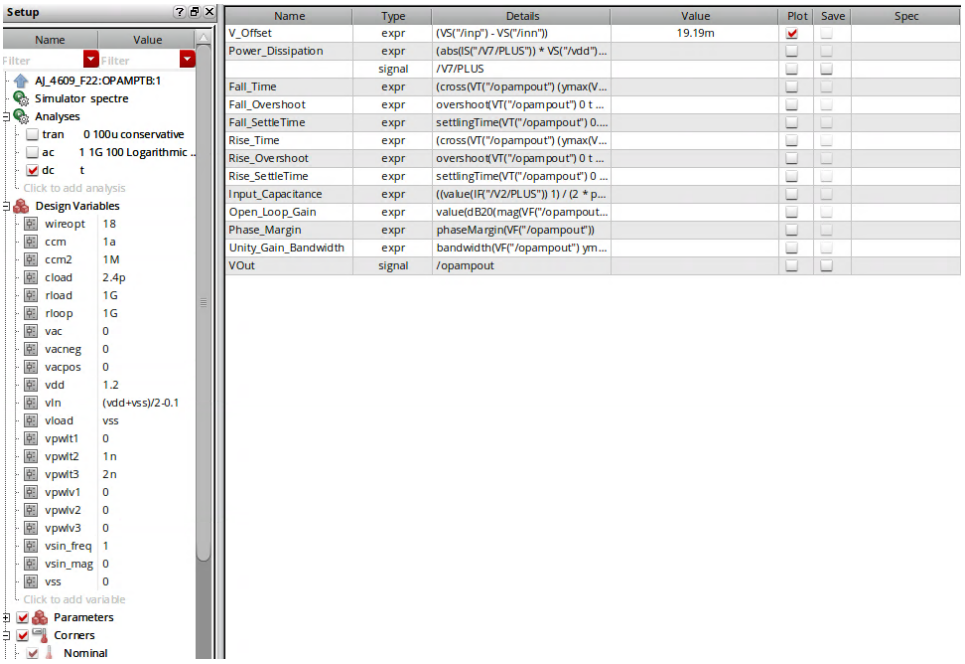


Figure 3.8: V offset under normal conditions.

Risetime (10%-90%):
1.277us

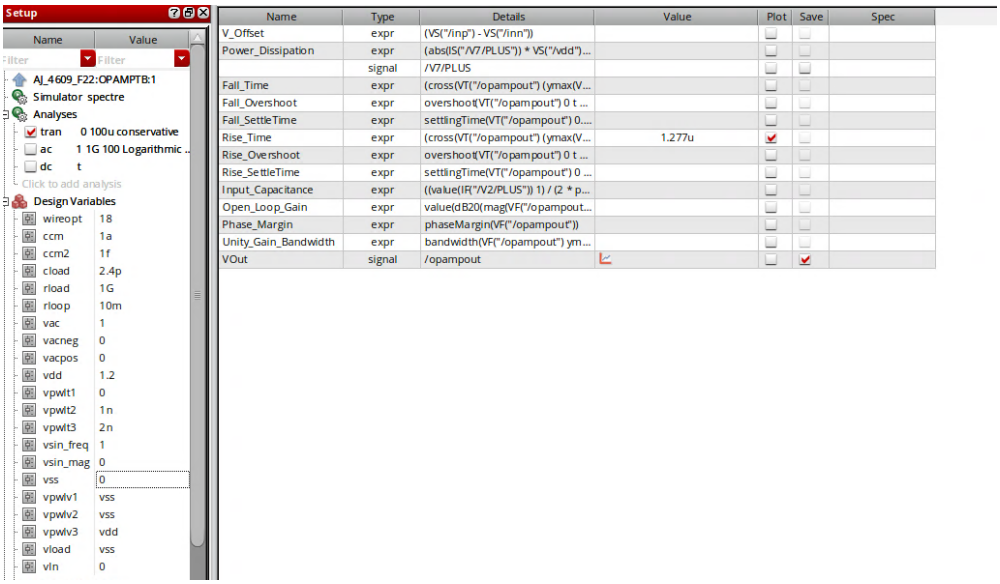


Figure 3.9: Rise time under normal conditions.

Falltime (10%-90%):

192.1ns

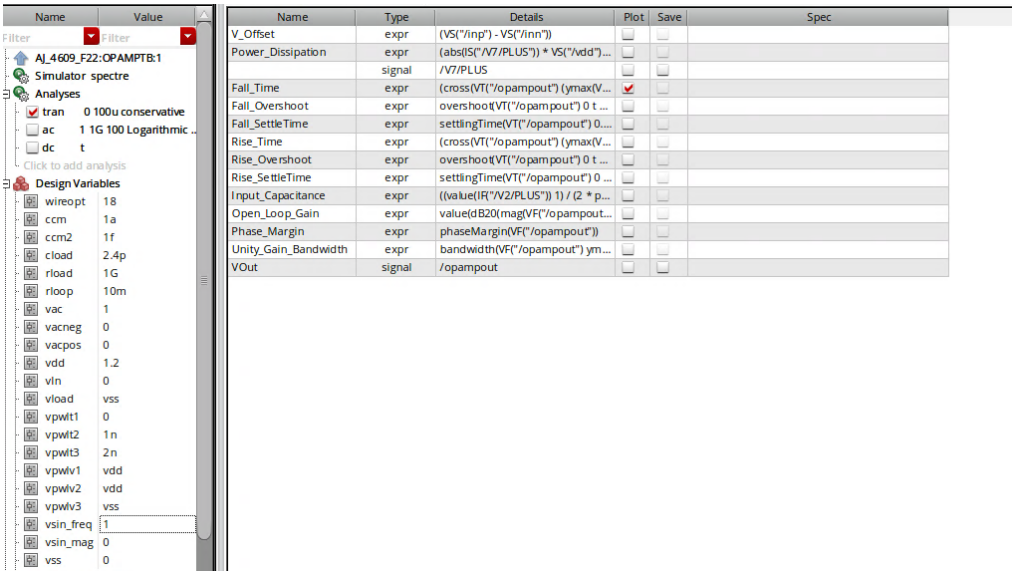


Figure 3.10: Fall time under normal conditions.

Following these results we will resimulate the PVT (Processes, Voltages, Temperatures) variations. There will be a total of 27 data points.

The naming convention goes in the following order (Process, Voltage, Temperature)
F = Fast
N=Nominal
S= slow

For Voltages:
Nominal = 1.2V, Fast = N+10% = 1.32V, Slow = N-10% = 1.08V

For Temperature:
Nominal = 25°C, Fast = -40°C, Slow = 85°C

Fast process simulations:

OPEN LOOP GAIN

FFF:19.22
FFN:19.26
FFS:18.95
FNF:19.22
FNN:19.26
FNS:18.95
FSF:19.22
FSN:19.26
FSS:18.95

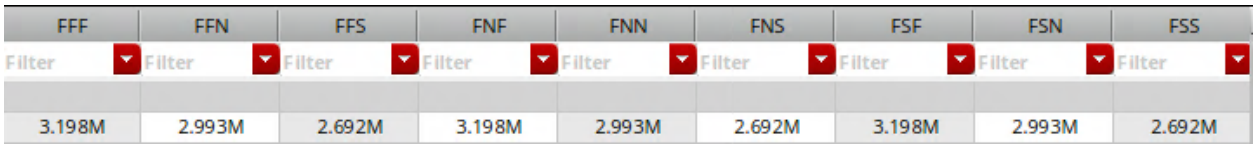
FFF	FFN	FFS	FNF	FNN	FNS	FSF	FSN	FSS
19.22	19.26	18.95	19.22	19.26	18.95	19.22	19.26	18.95

Figure 3.11: Open loop gain under fast process.

MAX = 20.38Ω
MIN = 18.95Ω

Unity Gain Bandwidth:

FFF: 2.993MHz
FFN:2.692MHz
FFS:3.198MHz
FNF:3.198MHz
FNN:2.993MHz
FNS:2.692MHz
FSF:3.198MHz
FSN:2.993MHz
FSS:2.692MHz



FFF	FFN	FFS	FNF	FNN	FNS	FSF	FSN	FSS
3.198M	2.993M	2.692M	3.198M	2.993M	2.692M	3.198M	2.993M	2.692M

Figure 3.12: Unity gain bandwidth under fast process.

MAX=3.198M
MIN= 2.043M

Phase Margin:

FFF: 106.3°
FFN:107.3°
FFS:108.3°
FNF:106.3°
FNN:107.3°
FNS:108.3°
FSF:106.3°
FSN:107.3°
FSS:108.3°

FFF	FFN	FFS	FNF	FNN	FNS	FSF	FSN	FSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
106.3	107.3	108.3	106.3	107.3	108.3	106.3	107.3	108.3

Figure 3.13: Phase margin under fast process.

MAX=110.8
MIN=106.3

Power Dissipation:

FFF: 1.202mW
FFN:1.205mW
FFS:1.128mW
FNF:1.202mW
FNN:1.205mW
FNS:1.128mW
FSF:1.202mW
FSN:1.205mW
FSS:1.128mW

FFF	FFN	FFS	FNF	FNN	FNS	FSF	FSN	FSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1.202m	1.205m	1.128m	1.202m	1.205m	1.128m	1.202m	1.205m	1.128m

Figure 3.14: Power dissipation under fast process.

MAX=1.205m
MIN=864.8u

Voffset:
FFF: 35.02mV
FFN:34.25mV
FFS:31.64mV
FNF:35.02mV
FNN:34.25mV
FNS:31.64mV
FSF:35.02mV
FSN:34.25mV
FSS:31.64mV

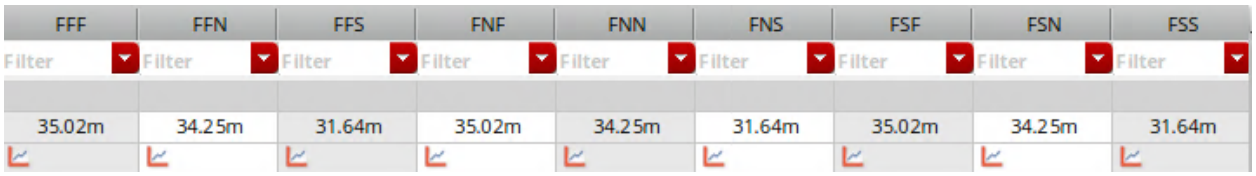


Figure 3.15: V offset under fast process.

MAX=35.02mV
MIN=19.19mV

Risetime (10%-90%):
FFF: 817.9ns
FFN: 681.8ns
FFS:654.1ns
FNF:817.9ns
FNN:681.8ns
FNS:654.1ns
FSF:817.9ns
FSN:681.8ns
FSS:654.1ns

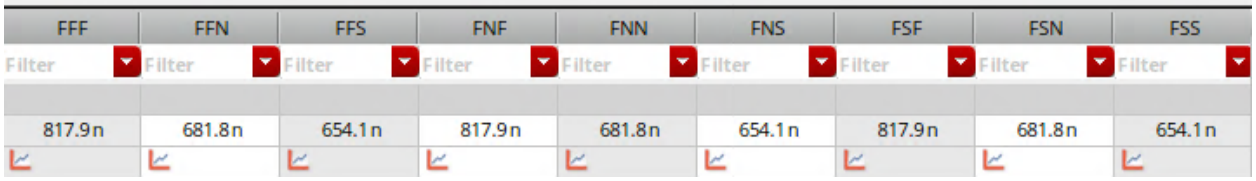


Figure 3.16: Rise time under fast process.

MAX=1.277us
MIN=654.1ns

Falltime (10%-90%):
FFF:120.6ns
FFN:132.5ns
FFS:155.7ns
FNF:120.6ns
FNN:132.5ns
FNS:155.7ns
FSF:120.6ns
FSN:132.5ns
FSS:155.7ns

FFF	FFN	FFS	FNF	FNN	FNS	FSF	FSN	FSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
120.6n	132.5n	155.7n	120.6n	132.5n	155.7n	120.6n	132.5n	155.7n

Figure 3.17: Fall time under fast process.

MAX= 192.1ns
MIN= 120.6ns

NOMINAL PROCESS SIMULATIONS:
OPEN LOOP GAIN

NFF: 20.23
NFN: 20.36
NFS:20.55
NNF:20.23
NNN:20.36
NNS:20.55
NSF:20.23
NSN:20.36
NSS:20.55

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
20.23	20.36	20.55	20.23	20.36	20.55	20.23	20.36	20.55

Figure 3.18: Open loop gain under nominal process.

MAX =20.55
MIN =20.23

Unity Gain Bandwidth:
NFF:2.173MHz
NFN: 2.034MHz
NFS:1.842MHz
NNF:2.173MHz
NNN:2.034MHz
NNS:1.842MHz
NSF:2.173MHz
NSN:2.034MHz
NSS:1.842MHz

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
2.173M	2.034M	1.842M	2.173M	2.034M	1.842M	2.173M	2.034M	1.842M

Figure 3.19: Unity gain bandwidth under nominal process.

MAX=2.173MHz
MIN=1.842MHz

Phase Margin:
NFF: 110.9°
NFN: 111.1°
NFS:111.9°
NNF:110.9°
NNN:111.1°
NNS:111.9°
NSF:110.9°
NSN:111.1°
NSS:111.9°

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
110.9	111.1	111.9	110.9	111.1	111.9	110.9	111.1	111.9

Figure 3.20: Phase margin under nominal process.

MAX=111.9°
MIN=110.8°

Power Dissipation::
NFF:858.8uW
NFN: 859uW
NFS:791.4uW
NNF:858.8uW
NNN:859uW
NNS:791.4uW
NSF:858.8uW
NSN:859uW
NSS:791.4uW

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
858.8u	859u	791.4u	858.8u	859u	791.4u	858.8u	859u	791.4u

Figure 3.21: Power dissipation under nominal process.

MAX=864.8uW
MIN=791.4uW

Voffset:
NFF: 18.32mV
NFN: 18.9mV
NFS:17.66mV
NNF:18.32mVV
NNN:18.9mV
NNS:17.66mV
NSF:18.32mV
NSN:18.9mV
NSS:17.66mV

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
18.32m	18.9m	17.66m	18.32m	18.9m	17.66m	18.32m	18.9m	17.66m

Figure 3.22: V offset under nominal process.

MAX=19.19mV
MIN=17.66mV

Risetime (10%-90%):

NFF: 1.584us
NFN: 1.294us
NFS: 1.201us
NNF:1.584us
NNN:1.294us
NNS:1.201us
NSF:1.584us
NSN:1.294us
NSS:1.201us

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
1.584u	1.294u	1.201u	1.584u	1.294u	1.201u	1.584u	1.294u	1.201u

Figure 3.23: Rise time under nominal process.

MAX=1.584us
MIN=1.201us

Falltime (10%-90%):

NFF: 188.5ns
NFN:193.2ns
NFS:225.5ns
NNF:188.5ns
NNN:193.2ns
NNS:225.5ns
NSF:188.5ns
NSN:193.2ns
NSS:225.5ns

NFF	NFN	NFS	NNF	NNN	NNS	NSF	NSN	NSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
188.5n	193.2n	225.5n	188.5n	193.2n	225.5n	188.5n	193.2n	225.5n

Figure 3.24: Fall time under nominal process.

MAX= 225.5ns
MIN=188.5ns

SLOW process simulations:

OPEN LOOP GAIN

SFF:20.85
SFN:20.94
SFS:21.25
SNF:20.85
SNN:20.94
SNS:21.25
SSF:20.85
SSN:20.94
SSS:21.25

SFF	SFN	SFS	SNF	SNN	SNS	SSF	SSN	SSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
20.85	20.94	21.25	20.85	20.94	21.25	20.85	20.94	21.25

Figure 3.25: Open loop gain under slow process.

Max =21.25
MIN = 20.38

Unity Gain Bandwidth:
SFF:1.887MHz
SFN:1.526MHz
SFS:1.369MHz
SNF:1.887MHz
SNN:1.526MHz
SNS:1.369MHz
SSF:1.887MHz
SSN:1.526MHz
SSS:1.369MHz

SFF	SFN	SFS	SNF	SNN	SNS	SSF	SSN	SSS
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1.887M	1.526M	1.369M	1.887M	1.526M	1.369M	1.887M	1.526M	1.369M

Figure 3.26: Unity gain bandwidth under slow process.

MAX=2.043MHz
MIN=1.369MHz

Phase Margin:

SFF:133.4°
SFN:125.5°
SFS:124.2°
SNF:133.4°
SNN:125.5°
SNS:124.2°
SSF:133.4°
SSN:125.5°
SSS:124.2°

SFF	SFN	SFS	SNF	SNN	SNS	SSF	SSN	SSS
133.4	125.5	124.2	133.4	125.5	124.2	133.4	125.5	124.2

Figure 3.27: Phase margin under slow process.

MAX=133.4°
MIN=110.8°

Power Dissipation:

SFF:604.5uW
SFN:613.8uW
SFS:565.3uW
SNF:604.5uW
SNN:613.8uW
SNS:565.3uW
SSF:604.5uW
SSN:613.8uW
SSS:565.3uW

SFF	SFN	SFS	SNF	SNN	SNS	SSF	SSN	SSS
604.5u	613.8u	565.3u	604.5u	613.8u	565.3u	604.5u	613.8u	565.3u

Figure 3.28: Power dissipation under slow process.

MAX=864.8uW
MIN=565.3uW

Voffset:
SFF:8.811mV
SFN:10.01mV
SFS:9.705mV
SNF:8.811mV
SNN:10.01mV
SNS:9.705mV
SSF:8.811mV
SSN:10.01mV
SSS:9.705mV

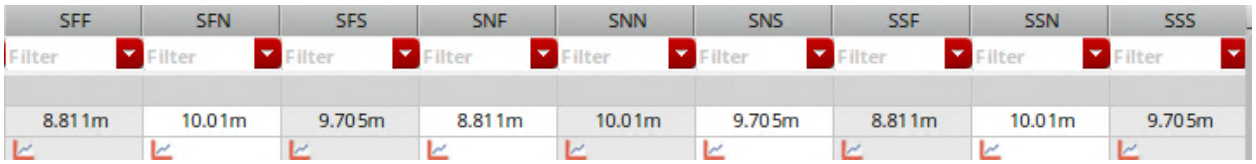


Figure 3.29: V offset under slow process.

MAX=19.19mV
MIN=8.811mV

Risetime (10%-90%):

SFF:2.802us
SFN:2.261us
SFS:1.993us
SNF:2.802us
SNN:2.261us
SNS:1.993us
SSF:2.802us
SSN: 2.261us
SSS: 1.993us

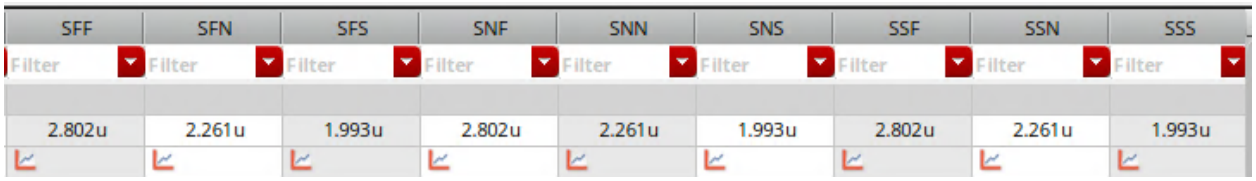


Figure 3.30: Rise time under slow process.

MAX= 2.802us
MIN= 1.277us

Falltime (10%-90%):
SFF: 285.6ns
SFN: 280.2ns
SFS: 317.9ns
SNF: 285.6ns
SNN: 280.2ns
SNS: 317.9ns
SSF:285.6ns
SSN: 280.2ns
SSS:317.9ns

Figure 3.31: Fall time under slow process.

Max = 317.9ns
MIN = 192.1ns

3.0 OP-AMP LAYOUT

Initially, we start by sectioning off the initial op-amp design based on restrictions. This will allow us to separate the given schematic into rows which we can create in layout.

The restrictions we must keep in mind:
PMOS transistors cannot be grouped with NMOS transistors. Inputs should remain paired therefore Q1 and Q2 must remain together. The output buffer should be either grouped or close together therefore Q8 and Q9 must be sectioned off. The differential-input first stage should remain together Q3 must remain with Q4. Finally The bias circuitry must remain together in one row therefore Q14, Q12, Q15 and Q13 should remain together.

Based on these restrictions the op-amp was sectioned off into the four groups shown in the diagram below:

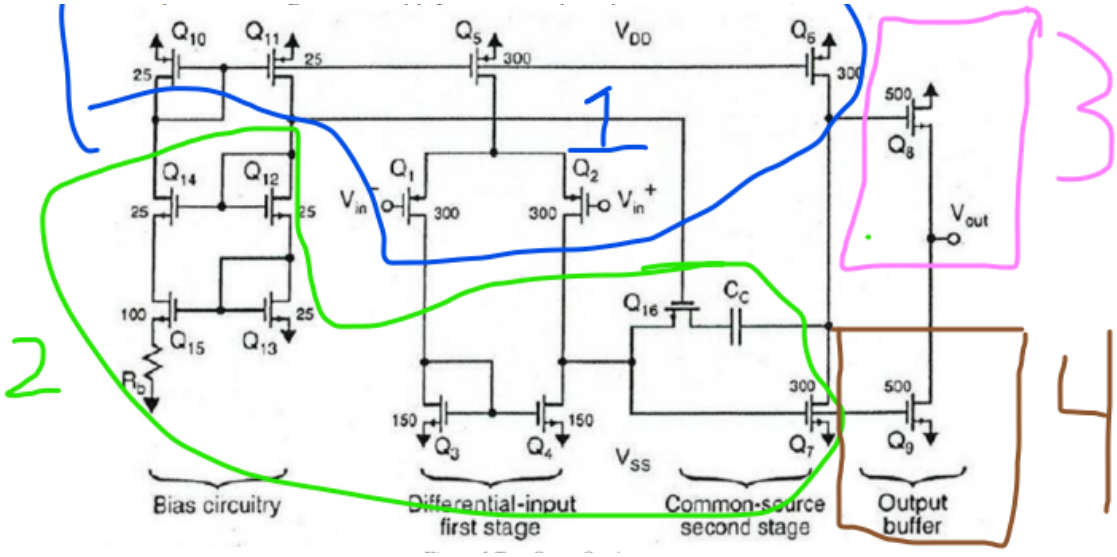


Figure 3.32: Op-Amp Layout Floor-plan sectioning

We decided to keep the PMOS transistors in one group following this we sectioned the current mirrors into the second group. Finally since transistors 3 and 4 have a large amount of fingers we split them into their own individual rows creating 4 rows in total.

Next, we must calculate the W/L ratios and decide on the amount of fingers as well as the individual finger width.

Total finger calculation for ROW 1 = Q1 + Q2 + Q5 + Q6+ Q10 + Q11 + . First we must decide on the width of the individual fingers should they be on the same row. Q10 and Q11 have a width of 1um therefore we must make the widths of the individual fingers of Q1, Q2, Q5 and Q6 the same size. Since they use the same finger width and amount of

fingers we can change the amount of fingers to 12 and therefore will have the same width.

The total amount of fingers = (12 X 4) + 2 = 50.

For the third and fourth row since they have the same amount of fingers and width then we are able to calculate how many fingers are needed to stay consistent. We opted to keep them at 50 fingers to remain symmetrical with row 1.

Now for row 2 we have gates Q3 + Q4 + Q7 + Q16 + Q12 + Q13 + Q14 + Q15. In this case we want to keep the width the same at 1um. Based on that we must change the amount of fingers to keep that constraint.

Based on the calculations done the new finger amounts become
Q3=Q4=6, Q16=1, Q7=12,Q14=Q12=Q13=1, Q15 = 4

Now calculating the total amount of fingers:
Q3 + Q4 + Q16 + Q7+Q14+Q12+Q13+Q15
= 6 + 6 + 1 + 12 + 3 + 4
= 32
To remain consistent we must add a minimum of 20 dummies.

Finally, we layout the calculated fingers symmetrically around the centre placing dummies to both keep the amount of fingers consistent while also ensuring two transistors that do not share a common source net are not placed together. Based on the dummies added the total amount of fingers was changed to 54. Therefore each row has a total of 54 transistors and dummies.

Layout Floor Plan

0 = 10, Z = 11, D = Dummy

66 55 66 55 66 55 D 11 22 11 22 11 22 D 0	Z D 22 11 22 11 22 11 D 55 66 55 66 55 66

D 88 99 88 99 88 99 88 99 88 99 88 99 88	99 88 99 88 99 88 99 88 99 88 99 88 99 D

D 88 99 88 99 88 99 88 99 88 99 88 99 88	99 88 99 88 99 88 99 88 99 88 99 88 99 D

12=A, 13 = B, 14=C, 15= X, 16=Y

DDDDDDDDD 77 77 77 D 33 44 33 D XX CD	A D XX D B D 44 33 44 DY D77 7777DDDDD

4.0 LAYOUT SIMULATION

Figure 3.33 below shows the final OP-AMP layout design. It matches the layout floor plan shown above.

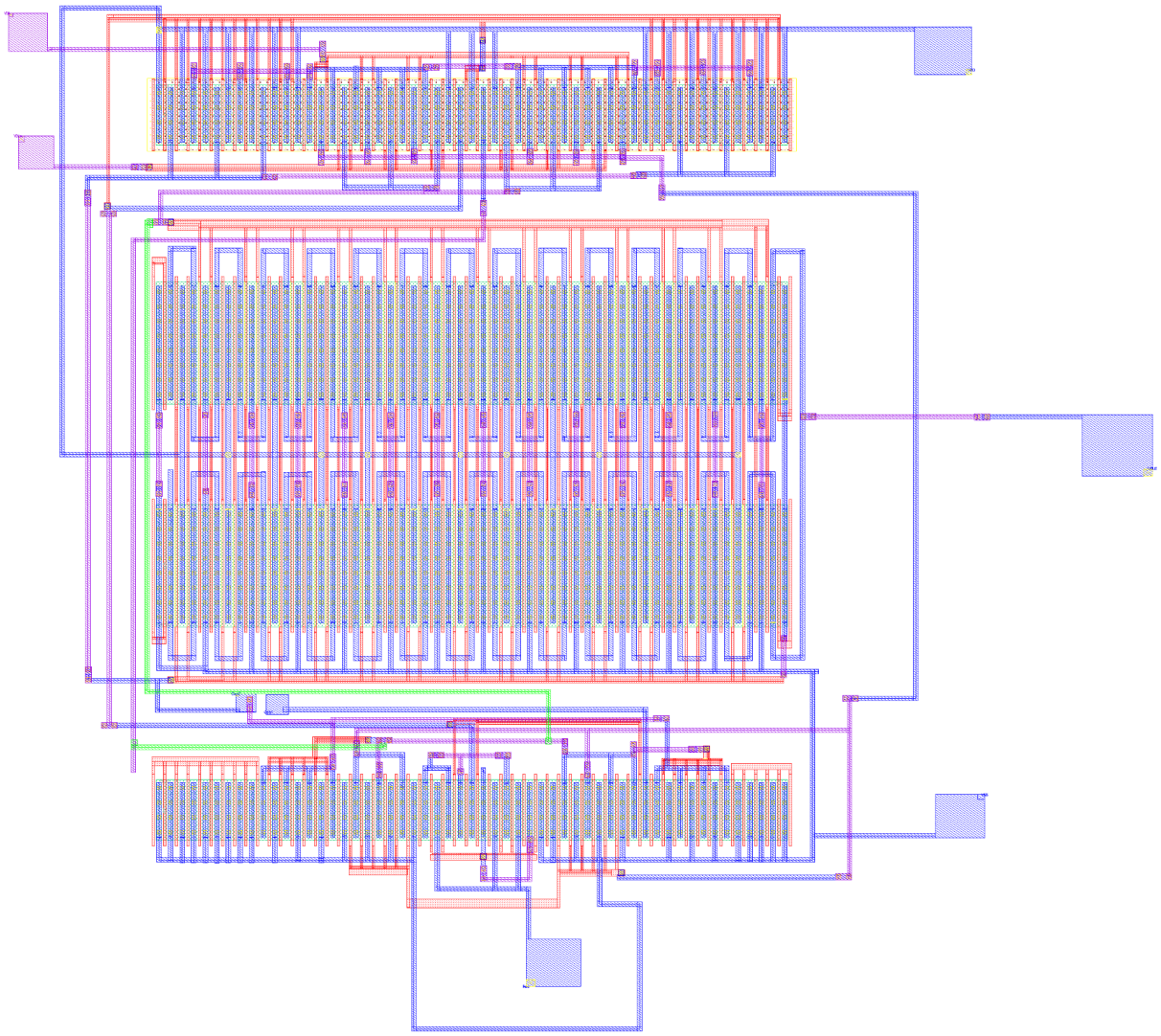


Figure 3.33: OpAmp layout design.

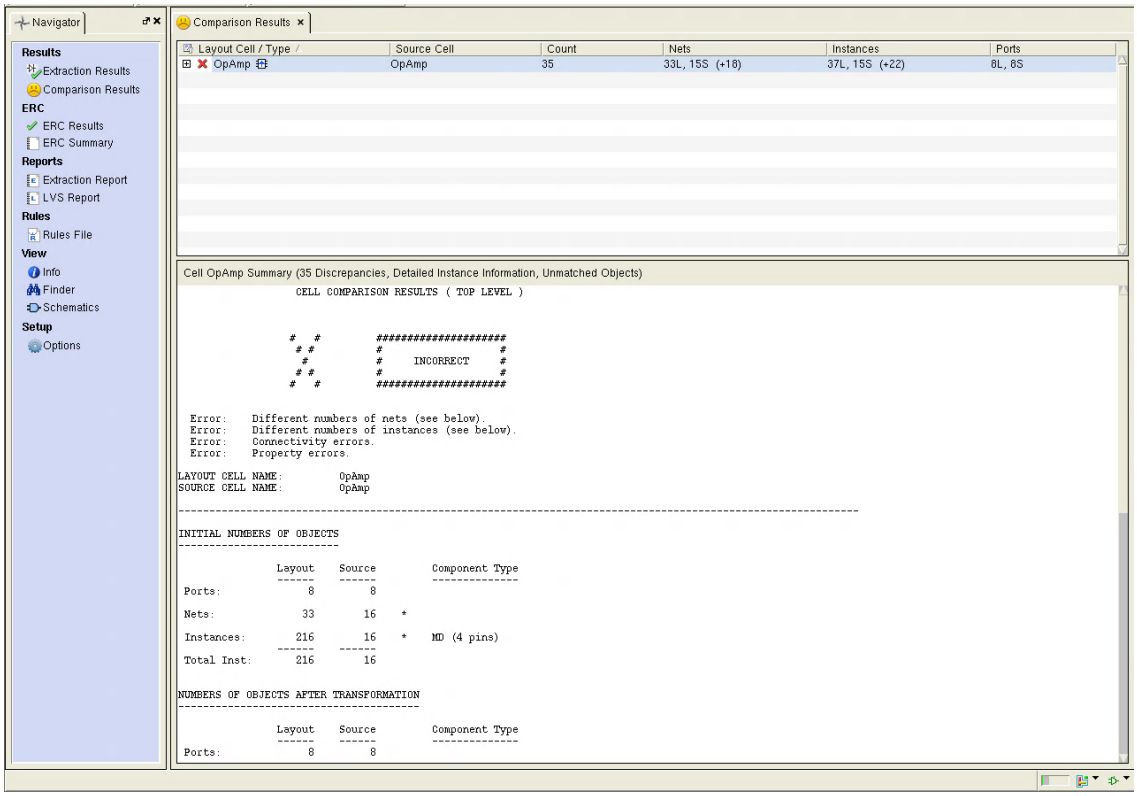


Figure 3.34: Layout LVS

Unfortunately, we were unable to fix all LVS errors and as a result couldn't run the required simulations.

Chapter 4: Group Member Contributions

1.0 CuSOI Schematics & Simulation:

Hussin Created the schematics and testbenches for the XNOR_RESET, Oscillator, D-flip-Flop, Output-Driver and the full top level static PRSG. Theo created the schematics and testbenches for the NAND gate, NOR gate, PRSG, and Input-Protection.

However, since the top level test-bench for the entire static PRSG was more difficult than anticipated, Theo helped in the creation of the testbench.

2.0 CuSOI Layout

Hussin and Theo both worked on the creation of the individual logic gates NAND and NOR. Hussin created the initial layout, and Theo utilised them to create a more space efficient version. Hussin created the layout for the input-protection, output-driver, oscillator and PRSG. Theo created the D-FlipFlop, XNOR_Reset and inverter. Although the overall top level full static PRSG was completed by both, Theo provided more input and took the lead towards its connections and completion.

3.0 CuSOI Report

The CuSOI report was almost entirely done by Theo with Hussin adding references and images where required as well as cleaning it, editing, and adding figure numbers prior to submission.

4.0 OpAmp Schematics & OpAmp PVT Simulations

The opAmp schematic and PVT simulations were done mostly by Hussin Abdullah with Theo providing input and help whenever needed

5.0 OpAmp Layout

The top level layout floor plan was created entirely by Hussin with theo providing input and assistance whenever required. The overall layout was completed by Theo with Hussin providing input and help whenever required.

6.0 OpAmp Report

The OpAmp report was written entirely by Hussin Abdullah

7.0 General Report Writing

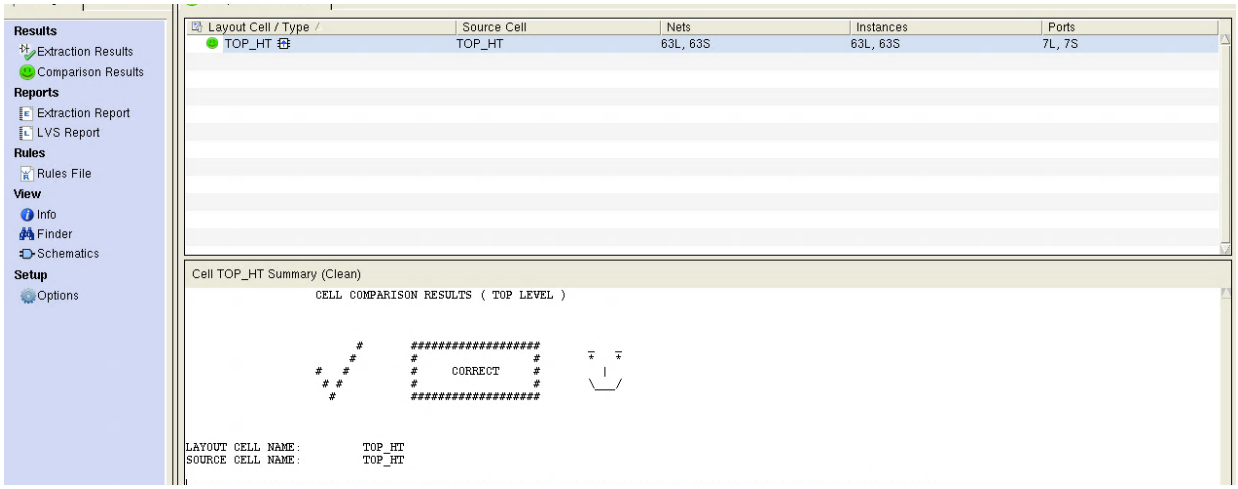
The report was split evenly with editing and figures added by both figures.

APPENDIX:

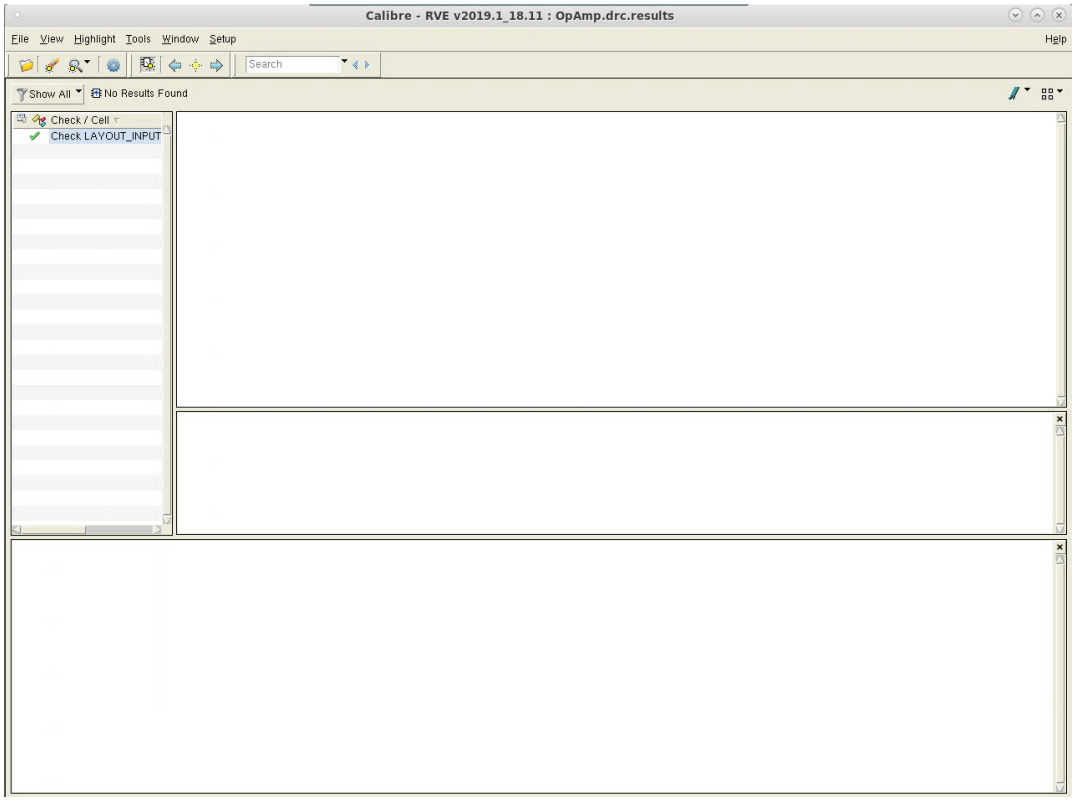
1. STATIC PRSG final DRC for Layout:

```
--- RULECHECK RESULTS STATISTICS
---
RULECHECK METAL_WIDTH ..................... TOTAL Result Count = 0 (0)
RULECHECK METAL_SPACING ................... TOTAL Result Count = 0 (0)
RULECHECK POLY_WIDTH ...................... TOTAL Result Count = 0 (0)
RULECHECK POLY_SPACING .................... TOTAL Result Count = 0 (0)
RULECHECK FIELD_POLY_DWELL_SPACING ........ TOTAL Result Count = 0 (0)
RULECHECK FIELD_POLY_SOURCE_DRAIN_TOUCHING ... TOTAL Result Count = 0 (0)
RULECHECK DWELL_WIDTH ..................... TOTAL Result Count = 0 (0)
RULECHECK DWELL_SPACING ................... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_WIDTH ................... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_METAL_OVERLAP ........... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_POLY_OVERLAP ............ TOTAL Result Count = 0 (0)
RULECHECK CHANNEL_CONTACT_SPACING ......... TOTAL Result Count = 0 (0)
RULECHECK CONTACT_D_WELL_OVERLAP .......... TOTAL Result Count = 0 (0)
RULECHECK NWELL_DWELL_OVERLAP.1 ........... TOTAL Result Count = 0 (0)
RULECHECK NWELL_DWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_NWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_P_SOURCE_DRAIN_ENCLOSURE ..... TOTAL Result Count = 0 (0)
RULECHECK Pplus_DWELL_OVERLAP.2 ........... TOTAL Result Count = 0 (0)
RULECHECK Pplus_N_SOURCE_DRAIN_SPACING ..... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK BAD_GATE.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK Grid.1 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.2 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.3 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.4 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.5 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.6 .......................... TOTAL Result Count = 0 (0)
RULECHECK Grid.7 .......................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_METAL .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_POLY ..................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_DWELL .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_NPLUS .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_PPLUS .................... TOTAL Result Count = 0 (0)
RULECHECK ART_TO_CONTACT .................. TOTAL Result Count = 0 (0)
RULECHECK ART_TO_NWELL .................... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 747 (2145)
TOTAL DRC RuleChecks Executed:   36
TOTAL DRC Results Generated:     0 (0)
```

2. Static PRSG final LVS report for Layout:



3. OP AMP DRC for LAYOUT



4. OP AMP final LVS report for layout: